

# **EXHIBIT 1**

**IN THE UNITED STATES DISTRICT COURT  
FOR THE DISTRICT OF DELAWARE**

CORRIGENT CORPORATION,

Plaintiff,

v.

DELL TECHNOLOGIES INC. and DELL INC.,

Defendants.

C.A. No. 22-496 (RGA)

**JURY TRIAL DEMANDED**

CORRIGENT CORPORATION,

Plaintiff,

v.

ARISTA NETWORKS, INC.,

Defendant.

C.A. No. 22-497 (RGA)

**JURY TRIAL DEMANDED**

**DECLARATION OF ANDREW C. MAYO IN SUPPORT OF CORRIGENT  
CORPORATION'S OPENING CLAIM CONSTRUCTION BRIEF**

I, Andrew C. Mayo, hereby declare as follows:

1. I am a partner with the law firm of Ashby & Geddes, counsel of record for Plaintiff Corrigent Corporation in this matter. I make this declaration from personal knowledge and, if called to testify, I could and would testify competently thereto.

2. Attached hereto as **Exhibit 1A** is a true and correct copy of an excerpt from the prosecution history for U.S. Patent No. 6,957,369, Response to Office Action, dated February 2, 2005.

3. Attached hereto as **Exhibit 1B** is a true and correct copy of excerpt from the prosecution history for U.S. Patent No. 6,957,369, Notice of Allowance, dated June 10, 2005.

4. Attached hereto as **Exhibit 1C** is a true and correct copy of *Corrigent Corp. v. Cisco Sys. Inc.*, 6:22-cv-00396-ADA (W.D. Tex.), Dkt. 69 (March 21, 2023).

5. Attached hereto as **Exhibit 1D** is a true and correct copy of *Corrigent Corp. v. Cisco Sys. Inc.*, 6:22-cv-00396-ADA (W.D. Tex.), Dkt. 49 (December 16, 2022).

6. Attached hereto as **Exhibit 2A** is a true and correct copy of the curriculum vitae of Dr. James Oliver.

7. Attached hereto as **Exhibit 2B** is a true and correct copy of U.S. Patent No. 5,420,985, issued on May 30, 1995.

8. Attached hereto as **Exhibit 2C** is a true and correct copy of RFC4026, *Provider Provisioned Virtual Private Network (VPN) Terminology*, dated March 2005.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Executed on January 9, 2024 in Wilmington, Delaware.

/s/ Andrew C. Mayo  
Andrew C. Mayo



# **EXHIBIT 1A**

DOCKET NO. 223756US



IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

BRUCKMAN et al. : GROUP: 2133

SERIAL NO: 10/156,851 : EXAMINER: KERVEROS, JAMES C

FILED: MAY 30, 2002 :

FOR: HIDDEN FAILURE DETECTION :

**AMENDMENT**

COMMISSIONER FOR PATENTS  
ALEXANDRIA, VIRGINIA 22313

SIR:

In response to the Office Action dated November 3, 2004, for the above-identified patent application, please consider the remarks below and amend the application as follows:

**Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

**Remarks** begin on page 11 of this paper.

### AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): In an electronic system that includes a main module and at least first and second subsidiary modules, each ~~such module~~ of said at least first and second subsidiary modules connected to the main module by one or more lines for carrying data, at least some of which lines ~~may be~~ are sometimes idle, the main module including a switch having ports connected to the lines, a method for self-testing the system, comprising:

selecting a first idle line among ~~the~~ idle lines connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid line;

instructing the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid line;

selecting for testing a second idle line among the idle lines connecting the second subsidiary module to a second port of the switch on the main module;

configuring the switch to link the first and second ports;

transmitting test traffic over the second idle line from the second subsidiary module to the main module, wherein the test traffic is conveyed via the switch to the aid line connecting to the first subsidiary module; and

reporting that a failure has occurred if the test traffic does not return to the second subsidiary module within a predetermined period of time.

Claim 2 (Currently Amended): A method according to claim 1, wherein instructing the first subsidiary module comprises configuring the first subsidiary module to loop back the

traffic to the main module substantially without processing the data comprised in the test traffic.

Claim 3 (Currently Amended): A method according to claim 2, wherein the first and second subsidiary modules are configured to transmit and receive the data in different, respective first and second formats, and wherein the test traffic transmitted from the second subsidiary module and looped back by the first subsidiary module is in the second format.

Claim 4 (Currently Amended): A method according to claim 1, ~~and~~ further comprising:

selecting one or more further idle lines for testing among the idle lines in the system, wherein the further idle lines connect to further ports of the switch on the main module; and  
repeating the ~~steps of~~ configuring the switch, transmitting the test traffic, and reporting that the failure has occurred with respect to the further idle lines until all the idle lines have been tested.

Claim 5 (Currently Amended): A method according to claim 1, wherein the main module and said at least first and second subsidiary modules comprise cards, which are plugged into a backplane, and wherein the lines comprise traces on the backplane.

Claim 6 (Original): A method according to claim 1, wherein the switch is configured to connect the lines to a network communication trunk, and wherein the traffic comprises communication traffic.

Claim 7 (Original): A method according to claim 6, wherein transmitting the test traffic comprises testing the second idle line while continuing to use the lines that are not idle for carrying the data to the network communication trunk.

Claim 8 (Currently Amended): In an electronic system that includes a main module and multiple subsidiary modules, each of said multiple subsidiary modules ~~such module~~ being connected to the main module by one or more lines for carrying data, a method for self-testing the system, comprising:

selecting first and second subsidiary modules of different types for testing among the multiple subsidiary modules, the first and second subsidiary modules being configured to transmit and receive the data in different, respective first and second formats;

instructing the first subsidiary module to loop back traffic reaching the first subsidiary module from the main module;

configuring the main module to connect the first and second subsidiary modules, so that the traffic transmitted by the second subsidiary module is conveyed to the first subsidiary module via the main module and is then looped back via the main module to the second subsidiary module; and

testing the system by causing the second subsidiary module to transmit test traffic in

the second format to the main module, and assessing whether the test traffic is returned intact from the first module.

Claim 9 (Currently Amended): A method according to claim 8, wherein instructing the first subsidiary module comprises configuring the first subsidiary module to loop back the traffic to the main module substantially without processing the data comprised in the test traffic.

Claim 10 (Original): A method according to claim 8, wherein the main module and subsidiary modules comprise cards, which are plugged into a backplane, and wherein the lines comprise traces on the backplane.

Claim 11 (Original): A method according to claim 8, wherein the main module comprises a switch, which is coupled to connect the lines to a network communication trunk, and wherein configuring the main module comprises configuring the switch to connect at least one of the lines of the first subsidiary module to at least one of the lines of the second subsidiary module.

Claim 12 (Original): A method according to claim 11, wherein testing the system comprises testing one or more of the lines of the second subsidiary module while continuing

to use at least some of the lines that are not under test for carrying the data from the subsidiary modules to the network communication trunk.

Claim 13 (Original): A method according to claim 8, wherein the traffic comprises communication traffic, and wherein the first and second formats are determined respectively by different first and second communication protocols.

Claim 14 (Original): A method according to claim 13, wherein one of the first and second protocols is a time domain multiplexing (TDM) protocol, while the other of the first and second protocols is a packet data protocol.

Claim 15 (Currently Amended): Modular electronic apparatus, comprising:

- a backplane, which comprises traces for carrying data between modules that are plugged into the backplane;
- a main module, ~~adapted to be~~ plugged into the backplane, the main module comprising a switch having ports for connection to the traces of the backplane;
- at least first and second subsidiary modules, ~~adapted to be~~ plugged into the backplane so as to be connected to the main module by the traces, at least some of which traces ~~may be~~ are sometimes idle; and
- a system control processor, which is ~~adapted~~ operative to select a first idle trace among ~~the~~ idle traces connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid trace, to instruct the first subsidiary module to loop back

traffic reaching the first subsidiary module via the aid trace, to select for testing a second idle trace among the idle traces connecting the second subsidiary module to a second port of the switch on the main module, and to configure the switch to link the first and second ports, the system control processor being further ~~adapted~~ operative to cause test traffic to be transmitted over the second idle trace from the second subsidiary module to the main module, wherein the test traffic is conveyed via the switch to the aid trace connecting to the first subsidiary module, and to report that a failure has occurred if the test traffic does not return to the second subsidiary module within a predetermined period of time.

Claim 16 (Currently Amended): Apparatus according to claim 15, wherein the first subsidiary module is configured, under control of the system control processor, to loop back the traffic on the aid trace to the main module substantially without processing the data comprised in the test traffic.

Claim 17 (Currently Amended): Apparatus according to claim 16, wherein the first and second subsidiary modules are configured to transmit and receive the data in different, respective first and second formats, and wherein the test traffic transmitted from the second subsidiary module and looped back by the first subsidiary module is in the second format.

Claim 18 (Currently amended): Apparatus according to claim 15, wherein the system control processor is ~~adapted~~ operative to select one or more further idle traces for testing among the idle traces in the system, wherein the further idle traces connect to further ports of

the switch on the main module, and to repeatedly configure the switch, cause the test traffic to be transmitted, and report the failure when it occurs with respect to the further idle traces until all the idle lines have been tested.

Claim 19 (Original): Apparatus according to claim 15, wherein the switch is configured to connect the traces to a network communication trunk, and wherein the traffic comprises communication traffic.

Claim 20 (Original): Apparatus according to claim 19, wherein the test traffic is transmitted over the second idle trace while continuing to use the trace that are not idle for carrying the data to the network communication trunk.

Claim 21 (Currently Amended): Modular electronic apparatus, comprising:

- a backplane, which comprises traces for carrying data between modules that are plugged into the backplane;
- a main module, ~~adapted to be~~ plugged into the backplane;
- a plurality of subsidiary modules, ~~adapted to be~~ plugged into the backplane so as to be connected to the main module by the traces; and
- a system control processor, which is ~~adapted~~ operative to select first and second subsidiary modules of different types for testing among the multiple subsidiary modules, the first and second subsidiary modules being configured to transmit and receive the data in different, respective first and second formats, and which is further ~~adapted~~ operative to test

the modules by causing the first subsidiary module to loop back traffic reaching the first subsidiary module from the main module, by configuring the main module to connect the first and second subsidiary modules, so that ~~the~~ a traffic transmitted by the second subsidiary module is conveyed to the first subsidiary module via the main module and is then looped back via the main module to the second subsidiary module, and by causing the second subsidiary module to transmit test traffic in the second format to the main module, and assessing whether the test traffic is returned intact from the first module.

Claim 22 (Original): Apparatus according to claim 21, wherein the first subsidiary module is configured to loop back the traffic to the main module substantially without processing the data comprised in the test traffic.

Claim 23 (Currently Amended): Apparatus according to claim 21, wherein the main module comprises a switch, which is coupled to connect the traces to a network communication trunk, and wherein the system control processor is ~~adapted~~ operative to configure switch to connect at least one of the lines of the first subsidiary module to at least one of the lines of the second subsidiary module during the test.

Claim 24 (Currently Amended): Apparatus according to claim 23, wherein the system control processor is ~~adapted~~ operative to test one or more of the traces connected to the second subsidiary module while at least some of the traces that are not under test continue

to be used for carrying the data from the subsidiary modules to the network communication trunk.

Claim 25 (Original): Apparatus according to claim 21, wherein the traffic comprises communication traffic, and wherein the first and second formats are determined respectively by different first and second communication protocols.

Claim 26 (Original): Apparatus according to claim 25, wherein one of the first and second protocols is a time domain multiplexing (TDM) protocol, while the other of the first and second protocols is a packet data protocol.

### REMARKS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-26 are presently active in this case. The present Amendment amends Claims 1-5, 8-9, 15-18, 21 and 23-24.

The outstanding Office Action objected to Claims 15-26 because of informalities. Claims 1-20 were rejected under 35 U.S.C. § 112, second paragraph, as indefinite. Claims 1-4, 6-9 and 11-14 were rejected under 35 U.S.C. § 102(b) over Serikawa et al. (U.S. Patent 6,028,845, herein referred as "Serikawa"). Claims 5, 10 and 15-26 were rejected under 35 U.S.C. § 103(a) over Serikawa in view of Bright et al. (U.S. Patent 5,541,862, herein "Bright").

Initially, Applicant respectfully requests that the reference WO 01/93499 cited in the Information Disclosure Statement filed November 13, 2002 be acknowledged as having been considered in the next Office Action. Copies of the reference WO 01/93499 and of the PTO-1449 form citing the reference filed on November 13, 2002 are submitted herewith.

Applicant also wishes to thank the Examiner Kerveros for the courtesy of an interview granted to Applicant's representative, Sanford T. Colb (Reg. No. 26,856), held in the U.S.P.T.O. on January 11, 2005. At the interview, Mr. Colb presented a proposed amendment to Claim 1 and argued the patentability of Claim 8 as filed. It was agreed that the proposed amendment overcomes the cited references, and that the examination of the application is subject to further search. It was also agreed that amending the preamble of Claims 1 and 8 to recite "a method for self-testing the system" and amending Claim 1 to state that "at least some of [the] lines are sometimes idle" would overcome the rejection of these

claims under 35 U.S.C. 112, second paragraph. In accordance with the interview, the present response amends Claims 1 and 8 in the present response, and amends Claim 15 similar to the amendment of Claim 1.

In response to the objection to Claims 15-26 for informalities, Claims 15, 18, 21, 23 and 24 are amended to remove the term "adapted to." Furthermore, Claims 1-5, 8-9, 15-17 and 21 are amended to correct minor formalities on antecedent basis. In light of the formal nature of these changes to the claims, the changes do not raise a question of new matter.

In response to the rejection of Claims 1-20 under 35 U.S.C. § 112, second paragraph, the preamble of Claims 1 and 8 are amended to recite "a method for self-testing the system," as agreed in the interview with the Examiner. Furthermore, the Claims 1 and 15 are amended to replace "may be" with "are sometimes," also as agreed in the interview. In view of the amendment to Claims 1, 8 and 15, it is believed that all pending claims are definite and no further rejection on that basis is anticipated. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work with the Examiner in a joint effort to derive mutually acceptable language.

In response to the rejection of Claims 1-4, 6-9 and 11-14 under 35 U.S.C. § 102(b), Claim 1 is amended to recite "wherein the test traffic is conveyed via the switch to the aid line connecting to the first subsidiary module." This feature finds non-limiting support in the disclosure as originally filed, for example at page 13, lines 18-25. The changes to Claim 1 clarify that claim over Serikawa. Therefore, the rejection is believed to be overcome and Applicant respectfully traverses the rejection of Claims 1-4, 6-9 and 11-14 and requests reconsideration of this rejection, as next discussed.

Briefly recapitulating, Claim 1 recites a method for self-testing that uses a switch in a

main module and two different subsidiary modules, which are connected to the main module and exchange test traffic via the switch.<sup>1</sup> A non-limiting example of the claimed test configuration is shown in Fig. 1 of the present application. The test traffic traverses a second idle line (trace 38 in this example) from a second subsidiary module (MODULE A), via the switch to a first idle line (trace 40) connecting to a first subsidiary module (MODULE K). The first subsidiary module, if it is operating properly, loops the traffic back through the switch to the second subsidiary module.<sup>2</sup> As recited in the specification at page 1, lines 17-23, the method permits the system to test its various idle lines and components flexibly, without intruding on normal traffic.

The applied reference Serikawa describes a communication-line-quality measuring system for use in a network configuration that includes transmission and terminal equipment. The network configuration is shown in Serikawa's Fig. 1, while the quality measuring system is shown in Fig. 10. As shown in this figure, TDMA equipment 11 sends signals over a down-link line to terminal equipment 12, which then loops the signals back over an up-link line to the terminal equipment.<sup>3</sup> Comparing device 73 in the TDMA equipment checks the returned signals against the original transmitted signal. The entire measurement process takes place between one TDMA equipment and one terminal equipment, without the test traffic passing through Serikawa's switching system 10. Serikawa is silent about transmitting test traffic between two different instances of terminal equipment (such as equipment 12 and 12a)<sup>4</sup> or between two different instances of TDMA equipment (such as 11 and 11a).

Therefore, Serikawa ***does not teach or suggest*** transmitting test traffic for loopback

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<sup>1</sup> See for example Applicant's specification in Fig. 1.

<sup>2</sup> See Applicant's specification from page 12-13.

<sup>3</sup> See Serikawa, for example at column 12, lines 1-16 and in Fig. 10.

<sup>4</sup> See Serikawa, for example in Fig. 1

via a switch, as claimed. Diverting the test traffic to the switch in Serikawa's system would simply not make sense. Therefore, amended Claim 1 is believed to overcome the rejection based on the Serikawa reference. Since Claims 2-4, 6 and 7 depend upon Claim 1, which is believed to be patentably distinct over the prior art, the rejection of dependent Claims 2-5, 6 and 7 is believed to be overcome.

Furthermore, Claim 8 recites a method for self-testing using first and second subsidiary modules *of different types*, which transmit and receive data in *different respective formats*. The outstanding Office Action appears to have not considered this limitation in rejecting Claim 8 on the same grounds as Claim 1. In Serikawa's system both TDMA equipment 11 and terminal equipment 12 include frame assembling and disassembling means.<sup>5</sup> The TDMA equipment and terminal equipment must therefore transmit and receive data in the same format, or else the frame assembling and disassembling mechanism will not work. Furthermore, Claim 8 also recites transmitting test traffic between the first and second subsidiary modules via a main module. The outstanding Office Action appears to have not considered this limitation recited in Claim 8, as well.

The combination of features recited in Claim 8 underscores the flexibility afforded by the invention recited therein to choose any pair of subsidiary modules to connect and test through the main module, regardless of whether the subsidiary modules are of the same or different types. Serikawa *neither teaches nor suggests* these features. Therefore, Serikawa fails to teach or suggest every feature recited in the noted claims, so that Claims 1-4, 6-9 and 11-14 are believed to be patentably distinct over the prior art. Accordingly, Applicant

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<sup>5</sup> See Serikawa, for example in Fig. 10

respectfully traverses, and requests reconsideration of, the rejection based on the Serikawa patent.<sup>6</sup>

In response to the rejection of Claims 5, 10 and 15-26 under 35 U.S.C. § 103(a), Claim 15 is amended in accordance with the changes to Claim 1 to recite "wherein the test traffic is conveyed via the switch to the aid trace connecting to the first subsidiary module." This feature finds non-limiting support in the disclosure as originally filed, for example at page 13, lines 18-25. The changes to Claim 15 clarify that claim over Serikawa in view of Bright. Accordingly, Applicant respectfully traverses the rejection of Claims 5, 10 and 15-26 and requests reconsideration of this rejection, as next discussed.

Claim 15 recites a modular electronic apparatus comprising a backplane, a main module, and at least first second subsidiary modules, all plugged into the backplane. A system control processor selects first and second idle traces on the backplane that connect the first and second subsidiary modules to first and second ports of a switch in the main module. The processor configures the switch to link the first and second ports and to cause test traffic to be transmitted from the second subsidiary module over the second idle trace to the main module.

As discussed above, the applied reference Serikawa *does not teach or suggest* a feature related to the claimed test traffic conveyed via the switch to the aid trace connecting to the first subsidiary module. Applicant respectfully submits that the applied reference Bright also *does not disclose* such a feature, as discussed next.

Bright describes an emulator and digital signal analyzer. To test the functional and

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<sup>6</sup> See MPEP 2131: "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," (Citations omitted) (emphasis added). See also MPEP 2143.03: "All words in a claim must be considered in judging the patentability of that claim against the prior art."

parametric characteristics of a unit without overloading a host computer, the host computer downloads a testing program to a plurality of digital signal processor modules. These modules perform functional environmental emulation data generation and analysis of the data received from the unit under test.<sup>7</sup> As explained above in reference to Claim 1, Serikawa does not teach or suggest transmitting test traffic for loopback via a switch, as required in Claim 15. Bright also fails to teach or suggest such an approach. Accordingly, Claim 15 is believed to be patentably distinct over the applied references. Since Claims 16-20 depend upon Claim 15, the rejection of these claims is believed to be overcome.

Furthermore, Claim 21 recites a modular electronic apparatus comprising a backplane, a main module, and a plurality of subsidiary modules, all plugged into the backplane. A system control processor selects for testing first and second subsidiary models of different types, which transmit and receive data in different respective formats. As explained above in reference to Claim 8, Serikawa does not teach or suggest this limitation. Bright similarly fails to teach or suggest apparatus with this capability. Therefore, Claim 21 is believed to be patentable over the cited references. Since Claims 22-26 depend upon independent Claim 1, these claims are also believed to be patentably distinct over the applied references.

Since Claim 1, upon which Claim 5 depends, and since Claim 8, upon which Claim 10 depends, are believed to be patentably distinct over the prior art as discussed above, the rejections of Claims 5 and 10 are also believed to be overcome. Even if the combination of Bright and Serikawa is assumed to be proper, neither of these references teach nor suggest the features of independent Claims 1 and 8.

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<sup>7</sup> See Bright, for example in the Abstract.

Application No. 10/156,851  
Reply to Office Action of November 3, 2004

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 1-26 is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact Applicant's undersigned representative at the below listed telephone number.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,  
MAIER & NEUSTADT, P.C.



Gregory J. Maier  
Attorney of Record  
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# **EXHIBIT 1B**



# UNITED STATES PATENT AND TRADEMARK OFFICE

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## NOTICE OF ALLOWANCE AND FEE(S) DUE

22850 7590 06/10/2005

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EXAMINER

KERVEROS, JAMES C

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 06/10/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/156,851	05/30/2002	Leon Bruckman	223756US2	7672

TITLE OF INVENTION: HIDDEN FAILURE DETECTION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$300	\$1000	09/12/2005

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. **PROSECUTION ON THE MERITS IS CLOSED.** THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. **THIS STATUTORY PERIOD CANNOT BE EXTENDED.** SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

### HOW TO REPLY TO THIS NOTICE:

#### I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER:** Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

# **PART B - FEE(S) TRANSMITTAL**

Complete and send this form, together with applicable fee(s), to: **Mail**

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**INSTRUCTIONS:** This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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22850 7590 06/10/2005

**OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT,  
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ALEXANDRIA, VA 22314**

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/156,851	05/30/2002	Leon Bruckman	223756US2	7672

TITLE OF INVENTION: HIDDEN FAILURE DETECTION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$300	\$1000	09/12/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
KERVEROS, JAMES C	2133	714-716000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 \_\_\_\_\_
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 \_\_\_\_\_
- 3 \_\_\_\_\_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

- ☐ Issue Fee
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5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature \_\_\_\_\_

Date \_\_\_\_\_

Typed or printed name \_\_\_\_\_

Registration No. \_\_\_\_\_

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/156,851	05/30/2002	Leon Bruckman	223756US2	7672
22850	7590	06/10/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			KERVEROS, JAMES C	
			ART UNIT	PAPER NUMBER
			2133	

DATE MAILED: 06/10/2005

## Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 470 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 470 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571) 272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

# Notice of Allowability

Application No.

10/156,851

Examiner

JAMES C KERVEROS

Applicant(s)

BRUCKMAN ET AL.

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amendment filed 2/2/2005.
2. ☒ The allowed claim(s) is/are 1-26.
3. ☒ The drawings filed on 30 May 2002 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All b) ☐ Some\* c) ☐ None of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

## Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 2/2/05
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date \_\_\_\_\_
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

ALBERT DECADY  
SUPERVISOR  
BIOLOGY CENTER 2100

### **DETAILED ACTION**

This is a Notice of Allowance in response to Amendment filed 2/2/2005.

#### ***Allowable Subject Matter***

Claims 1-26 are allowed.

### **REASONS FOR ALLOWANCE**

The following is an examiner's statement of reasons for allowance:

The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention of a method for self testing an electronic system and a modular electronic apparatus recited in the independent claims. Furthermore, the claimed invention is patentably distinct over the prior arts of record in view of the proposed amendment, which is now incorporated in the claims, as agreed by the Examiner pending a search update, during a personal interview with Applicant's representative, Sanford T. Colb, held in the USPTO on January 11, 2005. It was agreed that the proposed amendment overcomes the cited references, and that the examination of the application is subject to further search.

Claim 1, recites inter alia, method steps of transmitting test traffic over the second idle line from the second subsidiary module to the main module, wherein the test traffic is conveyed via the switch to the aid line connecting to the first subsidiary module.

Claim 8, recites inter alia, method steps of selecting first and second subsidiary modules of different types for testing among the multiple subsidiary modules, the first and second subsidiary modules being configured to transmit and receive the data in different, respective first and second formats, and wherein, configuring the main module to connect the first and second subsidiary modules, so that the traffic transmitted by the second subsidiary module is conveyed to the first subsidiary module via the main module and is then looped back via the main module to the second subsidiary module.

Claim 15, recites inter alia, a system control processor, which is operative to select testing a second idle trace among the idle traces connecting the second subsidiary module to a second port of the switch on the main module, and to configure the switch to link the first and second ports, wherein the system control processor being further operative to cause test traffic to be transmitted over the second idle trace from the second subsidiary module to the main module.

Claim 21, recites inter alia, a system control processor, which is operative to select first and second subsidiary modules of different types for testing among the multiple subsidiary modules, the first and second subsidiary modules being configured to transmit and receive the data in different, respective first and second formats, and wherein, configuring the main module to connect the first and second subsidiary

modules, so that the traffic transmitted by the second subsidiary module is conveyed to the first subsidiary module via the main module and is then looped back via the main module to the second subsidiary module.

Consequently, independent claims 1, 8, 15 and 21 are allowed over the prior arts of record. Claims 2-7, 9-14, 16-20, 22-26 are directly or indirectly depended upon the independent claims and therefore are also allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

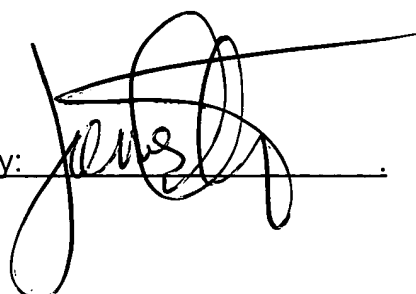
Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Randolph Building  
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Date: 5 April 2005  
Office Action: Allowance

By: 

JAMES C KERVEROS  
Examiner  
Art Unit 2133

  
ALBERT DECADY  
SUPERVISOR  
TECHNOLOGY CENTER 2100

# **EXHIBIT 1C**



**I. DISPUTED CONSTRUCTIONS:**

<b>Term No.</b>	<b>Term</b>	<b>Plaintiff's Proposed Construction</b>	<b>Defendant's Proposed Construction</b>	<b>Court's Final Construction</b>
1	<p>"idle line" '369 patent, claims 1, 3, 7</p> <p>"idle trace" '369 patent, claims 15, 18, 20</p>	Plain and ordinary meaning.	"a [trace/line] that is known to be inactive."	Plain and ordinary meaning.
2	<p>"subsidiary module" '369 patent, claims 1-3, 5, 8-12, 15-17, 17, 21-24</p>	Plain and ordinary meaning, which is a "module that has a connection to a main module via one or more data lines or traces."	"a module under the control of the main module."	Plain and ordinary meaning.
3	<p>"backplane" '369 patent, claims 5, 10, 15, 21</p>	Plain and ordinary meaning, which is "hardware used to establish interconnections between modules."	"a printed circuit board into which modules may be inserted."	Plain and ordinary meaning, which is "hardware used to establish interconnections between modules."
4	<p>Order of Steps '369 patent, claims 1, 8, 15, 21</p>	Plaintiff contends that Defendant's identification of the entirety of claim 1 and 8 for construction is improper. Plaintiff proposes that the words of claim 1 and 8 should be given the following meaning unless otherwise	The instruct[ing] step must be performed after the completion of the first selection; the configure[ing/e] step must be performed after the competition of both selections; and the transmit[ting] step must be performed after both selections.	The instruct[ing] step must be performed after the completion of the first selection; the configure[ing/e] step must be performed after the competition of both selections; and the transmit[ting] step must be performed after both selections.

		noted: plain and ordinary meaning.		
5	Preambles  '485 patent, claims 1, 11	Preambles are not limiting.	The preambles of claims 1 and 11 are limiting.	Preambles are not limiting.
6	"latency measurement packet"  '485 patent, all claims	"a packet that includes at least a subset of the fields showing in Table I of the '485 patent"	No construction necessary.	Plain and ordinary meaning, wherein the latency measurement packet contains at least some of the fields in Table I of the '485 patent.
7	"said FDB"  '400 patent, claims 1, 11	Plain and ordinary meaning.	Indefinite.	Not indefinite; plain and ordinary meaning, wherein "said FDB" means "said FDB of said first line card."
8	"virtual media access control (MAC) bridge"  '400 patent, claims 8, 11, 18	Plain and ordinary meaning, which is a media access control (MAC) bridge that serves a virtual private network (VPN) instance.	Indefinite.	Not indefinite; plain and ordinary meaning.
9	"RSVP-TE"  '602 patent, claims 3, 15	Plain and ordinary meaning.	"RSVP-TE protocol set forth in IETF RFC 3209."	"RSVP-TE protocol described in IETF RFC 3209."

10	Preamble  '602 patent, claim 15	Preamble is not limiting.	The preamble of claim 15 is limiting.	The preamble is not limiting.
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# **EXHIBIT 1D**

**IN THE UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF TEXAS  
WACO DIVISION**

CORRIGENT CORPORATION,

Plaintiff,

v.

CISCO SYSTEMS, INC.,

Defendant.

Case No. 6:22-cv-396-ADA-DTG

**DEFENDANT CISCO SYSTEMS, INC.'S REPLY CLAIM CONSTRUCTION  
BRIEF**

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**TABLE OF ABBREVIATIONS**

<b>Abbreviation</b>	<b>Definition</b>
'369 patent	U.S. Patent No. 6,957,369
'485 patent	U.S. Patent No. 7,113,485
'431 patent	U.S. Patent No. 7,330,431
'400 patent	U.S. Patent No. 7,593,400
'602 patent	U.S. Patent No. 9,119,602
Asserted Patents	U.S. Patent Nos. 6,957,369; 7,113,485; 7,330,431; 7,593,400; and 9,119,602
Corrigent	Plaintiff Corrigent Corporation
Cisco	Defendant Cisco Systems, Inc.
Ex.	Exhibit
Ke	U.S. Patent No. 5,841,788
Michalson Decl.	Rebuttal Declaration of Dr. William R. Michalson in Support of Defendant's Proposed Claim Constructions
Olivier Decl.	Declaration of Dr. James Olivier in Support of Corrigent's Responsive Claim Construction Brief

## TABLE OF EXHIBITS

Exhibit No.	Exhibit
Ex. A	<i>Idle</i> and <i>Subsidiary</i> , Collins English Dictionary, Harper Collins (5th ed. 2000) (CISCO_CORRIGENT-00001526)
Ex. B	<i>Idle</i> and <i>Subsidiary</i> , Random House Webster's Unabridged Dictionary 2d (2001) (CISCO_CORRIGENT-00001533)
Ex. C	<i>Subsidiary</i> , Funk & Wagnalls New International Dictionary of the English Language, World Publishers Inc. (2000) (CISCO_CORRIGENT-00001528)
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## I. '369 PATENT

### A. “idle line” (claims 1, 3, 7) / “idle trace” (claims 15, 18, 20)

As explained in Cisco’s opening brief, the specification, claims, and extrinsic evidence all demonstrate that a POSA would understand that an “idle [line/trace]” is a line/trace that is known to be inactive. Br. at 3–5. Corrigent’s arguments lay bare that it is attempting to read the word “idle” out the claims. Opp. at 1–4. Specifically, Corrigent states, without support, that an idle line refers to a line that is simply “ready for use.” *Id.* at 2. This blatant attempt to impermissibly broaden the claims is contrary to the well-understood meaning of “idle” and should be rejected as inconsistent with the claims and the specification. *See* Br. at 3–4; *see also Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1257 (Fed. Cir. 2010); *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 951 (Fed. Cir. 2006). The ’369 patent consistently distinguishes lines which are in use (active) and not in use (idle) and explains the importance of testing only lines not in use. Br. at 4. In fact, the stated purpose of the patent is to detect “hidden failures” on such lines. Br. at 1. Corrigent argues that Cisco’s construction imports a knowledge requirement into the claims. Opp. at 2. Not so. The claims themselves require that the line/trace be “idle” at the time of testing. *E.g.*, ’369 patent, cl. 1. The only way that can be ensured is to determine the line is idle before it is tested. Cisco’s construction used the word “known,” but could just as easily have used the word “determined” in its place, which would have had the same intended effect. The critical required feature of the ’369 patent’s use of the word “idle” is that the system tests a line only when it is detected to be idle. *See id.* at 1:11–15.

Though Corrigent objects to Cisco’s use of general dictionaries, “idle” is a commonly understood word and Corrigent does not allege there is a specialized technical meaning in the context of computer networking. Opp. at 3. General dictionaries are commonly used for nontechnical terms. *Praxair, Inc. v. ATMI, Inc.*, 543 F.3d 1306, 1325 (Fed. Cir. 2008) (allowing

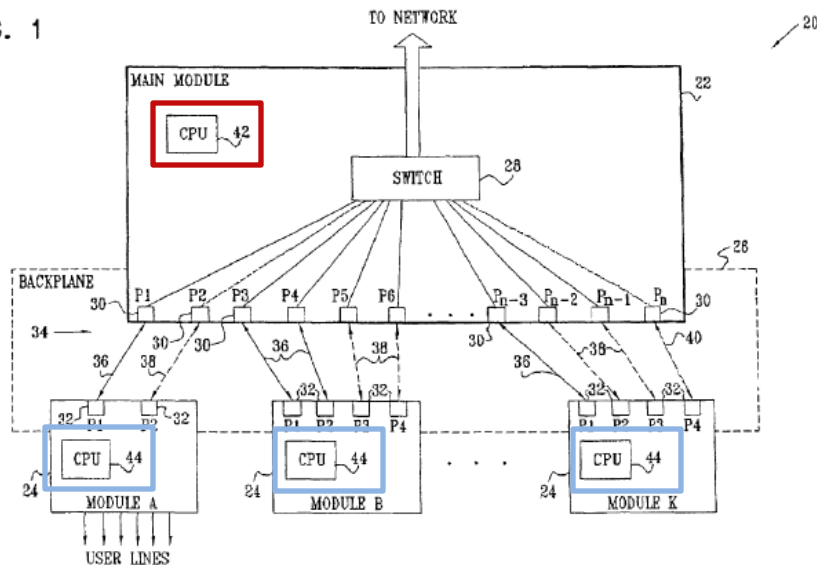
the use of the general dictionary in claim construction). Regardless, Cisco’s general dictionaries and Corrigent’s technical dictionary (which defines idle as “not being used, but ready”) are all in agreement—idle means inactive or not in use. *See* Exs. A–B, 7. Therefore, *AFG Industries, Inc. v. Cardinal IG Co., Inc.*, is irrelevant, as the court in *AFG Industries* disfavored the use of a general dictionary only because it was contrary to the definition in the technical dictionary. 239 F.3d 1239, 1248 (Fed. Cir. 2001).

**B. “subsidiary module” (claims 1–3, 5, 8–12, 15–17, 21–24)**

Cisco’s construction for “subsidiary module” appropriately reflects that a subsidiary module is under the control of a main module and not merely connected thereto. Br. at 2, 5–6. Corrigent seeks to improperly elide “subsidiary” entirely from the claims, arguing that the specification does not require a control relationship between the subsidiary module and main module. Opp. at 4. Corrigent’s argument ignores that the claims themselves require a “*subsidiary* module.” This a normal English word that means “secondary,” “assisting,” or “auxiliary,” all of which implies that it is under the control of a main system. Br. at 6. Corrigent does not provide any definition to the contrary or allege that there is a special technical meaning.

Corrigent insists that the system control processor, not the main module, controls the subsidiary module. Opp. at 5. This only proves Cisco’s point; the system control processor *is located in the main module*. Br. at 2. The patent states that “[t]he test procedure is supervised by an embedded system control processor **42** in main module 22.” ’369 patent at 5:41–45; Br. at 2. Figure 1 clearly shows the system control processor **42** inside the main module, while the subsidiary modules have general processors **44**. ’369 patent, Fig. 1; Br. at 2.

FIG. 1



'369 patent, Fig. 1; Br. at 2. To the extent the patent recites that the subsidiary may have a processor, that is not the system control processor. '369 patent at 1:33–36. Further, Corrigent's argument that a POSA would know that a system control processor could reside elsewhere in the system is a baseless attorney argument and has no support in the intrinsic record. *See Insituform Techs., Inc. v. Cat Contracting, Inc.*, 99 F.3d 1098, 1106 (Fed. Cir. 1996) (“[A]ttorney argument cannot control in light of the language of the claim.”).

### C. “backplane” (claims 5, 10, 15, 21)

Cisco's construction for “backplane” reflects what a POSA would understand a “backplane” to be: a printed circuit board into which modules are inserted. Br. at 8–10. In fact, Corrigent acknowledges the '369 patent's reference to “printed circuit traces on the backplane.” Opp. at 8 n.3.

The essence of Corrigent's argument is that the Court should ignore the specification's consistent use of the ordinary meaning of “backplane”—which is consistently recited in technical dictionaries, including one from the leading standards organization—in favor of Corrigent's self-serving expert testimony. Opp. at 9. This is both improper and incorrect. It is improper because

expert testimony cannot be used to contradict the intrinsic record. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005) (en banc) (“[A] court should discount any expert testimony that is clearly at odds with the claim construction mandated by the claims themselves, the written description, and the prosecution history, in other words, with the written record of the patent.”) (internal citation omitted). It is incorrect because Corrigent’s expert is mistaken. Opp. at 9. The Futurebus+’s backplane *is* a printed circuit board. Michalson Decl. ¶ 18. Any reference to “loosely” or “tightly coupled” in the description of Futurebus+ is referring to the architecture of the processors, not the backplane. *Id.* ¶¶ 18–23. In light of the ample evidence that a POSA would have understood that a backplane is a printed circuit board, the Court should adopt Cisco’s construction.

#### **D. Order of Steps (claims 1, 8, 15, 21)**

As explained in Cisco’s opening brief, the claim language itself requires the instructing step to be performed after the completion of the first selection, the configuring step must be performed after completion of both selections, and the transmitting step must be performed after both selections. Br. at 10–14. Despite Corrigent’s strawman, Cisco is *not* seeking to require all six recited steps to be performed in order.<sup>1</sup> Cisco seeks to impose only those order requirements that are mandated by the plain language of the claims. Corrigent admits that the transmitting step must be performed after the two selection steps (Opp. at 11), so that aspect of Cisco’s proposal seems undisputed. The only remaining disputes are (a) whether the instructing step must be performed after the completion of the first selection and (b) whether the configuring step must be performed after the completion of both selections.

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<sup>1</sup> Corrigent’s main argument is that each of the six steps do not need be performed in that exact order. Opp. at 10–12. That is a strawman because that is not Cisco’s proposal, as set forth above and in its opening brief. Br. at 10–14.

***The instructing step must occur after the first selection step.*** Corrigent argues that the instructing step can be performed at different times in the method, as long as it is before the “failures are checked.” Opp. at 11. This argument ignores the plain language of the claims. As explained in Cisco’s opening brief, the instructing step explicitly refers back to the results of the selecting step. Br. at 11. Without the prior selection, the subsidiary module would not know which line to use as an aid line, and the instruction would be meaningless. *Id.* Corrigent does not—and cannot—rebut this argument, and so it instead simply ignores the claim language.

***The configuring step must be performed after completion of both selections.*** Corrigent also fails to rebut Cisco’s argument that the configuring step must be performed after the selection of the aid line and idle line. As explained in Cisco’s opening brief, the configuring step explicitly refers to the aid and idle line—both of which were selected in the selecting steps—and thus must be performed only after the selections have occurred. Br. at 11. Without first selecting the lines connecting first and secondary subsidiary modules to the switch, it would be impossible to configure the switch to link the two lines. *Id.*

***The steps cannot be performed simultaneously.*** Corrigent’s arguments that the steps can occur simultaneously make no sense and, in any event, is unsupported by the intrinsic record. Corrigent relies entirely on the declaration of its expert, who merely opines that it is possible for the steps to be performed simultaneously if the steps in the claims are configuration settings. Olivier Decl. ¶ 25. This opinion lacks any support from the specification and should be disregarded. *Id.*; see *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1585 (Fed. Cir. 1996) (“Indeed, opinion testimony on claim construction, should be treated with utmost caution, for it is no better than opinion testimony on the meaning of statutory terms.”). Further, Corrigent’s reliance on *Kaneka* and *Ancora* is misplaced. In *Kaneka*, the specification explicitly

“contemplate[ed] continuous process steps.” *Kaneka Corp. v. Xiamen Kingdom Grp. Co.*, 790 F.3d 1298, 1306 (Fed. Cir. 2015). In contrast, the ’369 patent specification has no disclosure of a continuous process and instead recites a sequential process consistent with the claim language. *See generally* ’369 patent. Further, *Ancora* actually supports Cisco’s position. Opp. at 12. The Court in *Ancora* held that the claim language *required* that some steps be completed after other steps are completed. *Ancora Techs. Inc., v. LG Elecs. Inc.*, No. 20-cv-00034, 2020 WL 4825716, at \*5 (W.D. Tex. Aug. 19, 2020). Here, Cisco has shown above that the steps rely on the outcomes of the previous steps to begin and thus it would be impossible for the steps to be performed simultaneously. Br. at 11–14. It makes no sense for “selection” to somehow occur simultaneously with configuration and instruction when the latter two steps require the selection to have been made before they can occur.

***Order of steps applies to apparatus claims.*** In regard to claims 8 and 15, Corrigent argues that the order of steps does not apply to apparatus claims. Opp. at 12–14. This is incorrect. Corrigent’s own case supports Cisco’s position. In *Maxim Integrated Products, Inc. v. Silicon Mitus Tech., Inc.*, the court construed an order of steps in the apparatus claims because “courts will impose such a sequential order on an apparatus claim when the claim language contemplates and explicitly describes a sequential process, or when the disclosed system performs essentially similar steps as a method claim.” No. 17-cv-03507, 2018 WL 4657384, at \*9 (N.D. Cal. Jul. 3, 2018) (internal citation omitted). Here, the steps in method claims 1 and 8 are substantially similar to the sequential process in the apparatus claims 15 and 21, and therefore should be construed as a sequential process. *See* Br. at 12–14. Indeed, this Court recently applied the order of steps not only to the method claim but to apparatus claims that recited similar sequential steps for an apparatus to perform. *WSOU Investments LLC v. Dell Techs. Inc.*, No. 6:20–cv-00476-ADA, slip.

op. at 9 (W.D. Tex. May 27, 2021).

## II. '485 PATENT

### A. Preambles are limiting (claims 1, 11)

Corrigent's arguments actually support Cisco's position that the preambles should be limiting and fail to provide any reason why they should not.

First, without the preamble, there is no context for any of the recited steps of claim 1 or 11. Assuming *arguendo* that Corrigent's characterization of claim 1 and 11 is correct, the claim reduces to (1) transmitting a latency measurement packet "in *one direction* on a network," (2) transmitting that packet back "in a *second direction*," and (3) updating information in the latency measurement packet to calculate the latency. Opp. at 15. However, network topologies that are not ring networks generally have no concept of direction. Michalson Decl. ¶¶ 25, 28. A ring network is a unique topology where one node is connected to exactly two other nodes, and all the nodes connect to form a closed loop allowing traffic to travel either in a clockwise or counterclockwise direction. *Id.* ¶¶ 24–25. Other network types have many choices in how they route traffic through the network. *Id.* ¶ 26. Hence, a ring network is a unique type of network topology where direction matters. *Id.* ¶¶ 24–25. Without the context of the preamble, the claim elements asserting a first direction or a second direction would have no meaning because other network topologies have no concept of "direction," which is unique to ring topologies. *Id.* ¶ 28.

Second, Corrigent's argument that the present invention is not limited to ring networks, but may apply to other network types only further supports why the preamble should be limiting. Claims 1 and 11 specifically recite "a ring network," whereas independent claims 6, 9, 16, and 19 recite more generally "a network." Thus, claims 1 and 11 cover the preferred embodiment of the ring network, and claims 6, 9, 16 and 19 cover the other network types. "The doctrine of claim differentiation create[s] a presumption that each claim in a patent has a different scope." *Versa*

*Corp. v. Ag-Bag Int'l Ltd.*, 392 F.3d 1325, 1330 (Fed. Cir. 2004) (internal citation omitted). “The difference in meaning and scope between claims is presumed to be significant ‘[t]o the extent that the absence of such difference in meaning and scope would make a claim superfluous.’” *Id.* (quoting *Tandon Corp. v. U.S. Int'l Trade Comm'n*, 831 F.2d 1017, 1023 (Fed. Cir. 1987)). Corrigent fails to address this argument at all in its response. But as the Federal Circuit has stated, the difference is significant. Reading claims 1 and 11 to have the same scope as claims 6, 9, 16 and 19 would render the word “ring” in claims 1 and 11 superfluous, which would be contrary to the law.

Third, the recited “ring network” in the preamble provides antecedent basis for “the network” in the body of the claim. Otherwise, “the network” in the body of the claim would be indefinite. A claim is indefinite when it contains words or phrases where the meaning is unclear, which may be the result of the lack of an antecedent basis. *See In re Packard*, 751 F.3d 1307, 1310 (Fed. Cir. 2014). For claims 1 and 11, there is only one network recited in the claim—a ring network—and therefore, the antecedent basis for “the network” must be “a ring network.” Michalson Decl. ¶ 27. There is nothing else that could provide the antecedent basis. If the Court accepts Corrigent’s argument that “a ring network” does not provide antecedent basis for “the network,” then it should also find the term indefinite.

Finally, Corrigent’s argument regarding claim differentiation between an independent and dependent claim is incorrect. Claims 8, 10, 18 and 20 do not depend from claims 1 and 11, but rather depend from claims 6, 9, 16 and 19, respectively. Those independent claims do not recite “a ring network” in the preamble. Thus, claims 8, 10, 18 and 20 which narrow independent network-agnostic claims 6, 9, 16 and 19 to “ring networks” have no impact on claims 1 and 11. Because the preamble of claims 1 and 11 already limit those claims to a ring network, there is no

need for their dependent claims to narrow in this manner.

**B. “latency measurement packet” (all claims)**

A “latency measurement packet” (LMP) is a term readily understood in the art, and is not a coined term specific to the ’485 patent as Corrigent argues. In fact, the ’485 patent itself describes uses of LMPs when describing the prior art as Cisco argued in its opening brief. Br. at 19 (citing ’485 patent at 2:41–45). The fact that the ’485 patent describes the fields contained in an LMP does not mean an LMP can only be understood within the context of the ’485 patent. The only significance of Table I is to describe the fields that *may* be included in the LMP. Michalson Decl. ¶ 34. The ’485 patent states that Table I lists the fields “generally” contained in an LMP, and specifically that “[s]ome of the fields are optional,” but does not specify which fields. ’485 patent at 7:17–25. Unsurprisingly, Corrigent’s construction fails to articulate which fields are required by the LMP. Moreover, Corrigent changed its construction from requiring six fields to maybe requiring four fields. *Compare* Ex. I at 4, *with* Opp. at 19, 21 n.7. Corrigent’s own indecision and shifting positions further underscore why limiting this broad term to suit Corrigent’s litigation motives is inappropriate and unsupported. Corrigent’s difficulty in articulating a precise construction is because a latency measurement packet may include different fields depending on its function. *See* Opp. at 21 (arguing that certain fields are required by certain claims but not others).

Regardless, a POSA would understand the meaning of a latency measurement packet without needing a construction. Michalson Decl. ¶ 30. “Methods of network latency measurement are known in the art,” as the ’485 patent itself admits. *See* ’485 patent at 2:1–45. A data packet is also well known in the art. Michalson Decl. ¶ 32. Thus, a POSA would understand that a “latency measurement packet” is a packet that is used for latency measurement. *Id.* ¶ 33. Indeed, the plain

English language of the term compels such a conclusion. And as Corrigent already admitted, the fields of this packet change based on the packet's purpose. A POSA would know how to construct a data packet so that it may be used for its intended purpose, including that of the '485 patent. *Id.* ¶¶ 30–34.

### III. '400 PATENT

#### A. “said FDB” (claims 1, 11)

Corrigent's arguments make clear that it is not seeking a “plain and ordinary meaning” construction for “said FDB.” Instead, Corrigent seeks to rewrite the claim to refer to an FDB that is *not even recited in the claim*, by replacing “said FDB” with “said FDB of the first line card.”

Corrigent's primary argument hinges entirely upon its assertion that “plurality of conjoined member line cards” includes the “first and second line cards.” Opp. at 23–24. Contrary to Corrigent's insistence, however, *nothing in the claims requires the recited conjoined member line cards to include the first and second line cards*. This fact alone is enough to reject Corrigent's proposed construction because the claims simply do not recite any FDB on the first and second line cards. Thus, the term “said FDB” certainly cannot refer to an FDB on the first line card.

As shown above, not only are the recitations of “first and second line cards” and “plurality of conjoined member line cards” separate with no link between them, but they are recited in entirely different contexts. While the first configuring step recites a “first and second line card” in a “*network node*,” the second configuring step recites a “plurality of conjoined member line cards” that are part of a LAG group “*between two endpoints*.” There is nothing in this method claim that requires the “network node” be one of the claimed “endpoints,” or that the “first and second line cards” and the “conjoined line cards” are even in the same node. And, most critically, there is nothing in the claim to require the line cards recited on the “endpoints” be the *same ones* that are recited as part of the “network node.” Thus, the entire premise of Corrigent's argument,

*i.e.*, that the first and second line card are part of the conjoined member line cards, has no basis whatsoever in the claims.

Corrigent tries to avoid the claim language by arguing that the specification states that “the first and second line cards . . . are conjoined in a link aggregation (LAG).” Opp. at 24 (citing ’400 patent at 4:42–44). Corrigent, however, gives no justification for limiting the claim to a single embodiment in the specification, particularly where the claim language contradicts that disclosure in the specification. *See Phillips*, 415 F.3d at 1323 (“[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.”).

To the extent the claims do require the first and second line cards to be part of the conjoined member line cards—contrary to the claim language—Corrigent’s next argument is “said FDB” must refer to the FDB on the first line card because the previous limitation recites sending the packet “to at least said first line card.” Opp. at 23–24. Corrigent’s argument is misleading for two reasons. First, the claims do not recite an FDB on said “first line card,” so there is no recited “FDB” to which “said FDB” could refer. Instead, the claims recite “said FDB” without referring to which of the member line cards associated with an FDB the term refers. The claims, therefore, remain unclear to which FDB “said FDB” refers. Second, Corrigent’s argument hinges upon the steps being performed in order because it relies upon the use of “said first line card” in the previous limitation. Opp. at 23–24. Corrigent agrees that there are other FDBs recited elsewhere in the claim so, unless Corrigent stipulates to the receiving, conveying, and flooding limitations are performed in order, its argument is beside the point.

Corrigent argues that claim 11 is definite because it twice refers to “said FDB of said first line card” so a person of skill would understand the reference to “said FDB” refers to the same line

card. Opp. at 24–25. Not so. Although claim 11, unlike claim 1, does recite an FDB on the first line card, the prior references show that the patentee knew how to properly refer to a *specific* FDB, but does not excuse its failure to do so here. There are multiple FDBs to which it could refer. *See Bushnell Hawthorne, LLC v. Cisco Sys., Inc.*, 813 F. App’x 522, 526 (Fed. Cir. 2020); Br. at 23–24 (collecting cases). Indeed, the limitation immediately before refers to both the first line card and the second line card, so the same ambiguity arises in claim 11 as in claim 1. *See* ’400 patent at 12:47–53.

Finally, Corrigent wrongly faults Defendants for not providing expert testimony. Opp. at 24. But Corrigent’s own expert does nothing but repeat Corrigent’s arguments under the guise of an expert opinion without providing his own analysis. Olivier Decl. ¶¶ 32–36. For example, the first half of paragraph 34 of his declaration appears to be *copied word-for-word from Corrigent’s brief*. Compare Olivier Decl. ¶ 34, with Opp. at 23–24. Courts routinely discount expert testimony that fails to provide any analysis and instead only makes conclusory allegations regarding the legal conclusion. *See Phillips*, 415 F.3d at 1318 (“[C]onclusory, unsupported assertions by experts as to the definition of a claim term are not useful to a court.”). In any event, there is no requirement that an indefiniteness finding rest on expert testimony—especially where, as here, the term is ambiguous on its face and Corrigent’s own interpretation contradicts the rest of the claim language. *E.g., Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1370 n.6 (Fed. Cir. 2014) (holding it was “unnecessary to rely on [expert] testimony (or any other extrinsic evidence)” to reach the conclusion that the claims were indefinite). Cisco therefore respectfully requests this term be held indefinite.

#### **B. “virtual media access control (MAC) bridge” (claims 8, 11, 18)**

Corrigent and its expert do not dispute that “virtual MAC bridge” is a coined term without a well-understood meaning. *See* Opp. at 26–27; Olivier Decl. ¶¶ 37–38. This admission defeats

Corrigent’s request for “plain and ordinary meaning” because *there is no plain and ordinary meaning*. Because this is a coined term without a well-understood meaning, the intrinsic record must provide objective boundaries for that term. *See Iridescent Networks, Inc. v. AT&T Mobility, LLC*, 933 F.3d 1345, 1353 (Fed. Cir. 2019). It does not.

Corrigent argues that “virtual MAC bridge” should mean “media access control (MAC) bridge that serves a virtual private network (VPN) instance.” Opp. at 26. Corrigent relies exclusively on two parts of the intrinsic record to supply the required scope of the term: the wherein clause from claim 8 and substantially identical language in the specification. Opp. at 26–27. Corrigent is incorrect. If the term itself already had the same meaning as the language in the claim, then the “wherein” clause would be redundant. Such an interpretation is not correct. *See Digital-Vending*, 672 F.3d at 1275. This “wherein” language therefore fails to provide objective boundaries to what Corrigent itself admits is a coined term without a well-understood meaning. This case is no different than *IQASR*, which Corrigent fails to meaningfully distinguish. Opp. at 27. Cisco therefore respectfully requests this term be found indefinite.

#### **IV. ’602 PATENT**

##### **A. “RSVP-TE” (claims 3, 15)**

Corrigent’s assertion that Cisco’s proposed construction of “RSVP-TE” is “limited to a description contained in [IETF RFC 3209]” is a misleading strawman. *See* Opp. at 28. Cisco’s proposal does not exclude, for example, the “RSVP-TE protocol set forth in IETF RFC 3209” *as updated by* RFC 3936, because both documents *describe the same RSVP-TE protocol*. *See id.* (citing Ex. 4 and noting that RFC 3936 updates RFC 3209). Moreover, Cisco’s construction is consistent with the intrinsic record, which has but a single definitional statement indicating that “RSVP-TE” is the protocol “described by Awduche et al., in IETF RFC 3209.” ’602 patent at 1:46–50; *see, e.g., Bell Atl. Network Servs., Inc. v. Covad Commc’ns Grp., Inc.*, 262 F.3d 1258,

1271 (Fed. Cir. 2001) (“[W]hen a patentee uses a claim term throughout the entire specification, in a manner consistent with only a single meaning, he has defined that term ‘by implication.’”) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).

Corrigent’s attempt to broaden the scope of this term using extrinsic evidence is improper, because there is neither ambiguity nor uncertainty as to what the patentee meant by “RSVP-TE.” *See, e.g., Seabed Geosolutions (US) Inc. v. Magseis FF LLC*, 8 F.4th 1285, 1290 (Fed. Cir. 2021) (“Given the clarity of the intrinsic evidence, resort to extrinsic evidence is unnecessary.”). Regardless, Corrigent’s extrinsic evidence actually supports *Cisco*’s proposed construction. As noted above (and explained by Corrigent’s expert), RFC 3936 (Ex. 4) expressly updates RFC 3209, and therefore describes the same “well-known protocol” originally set forth in RFC 3209. Olivier Decl. ¶¶ 39–40. In addition, the Cisco publication’s chapter on “RSVP for Traffic Engineering and Fast Reroute” states that “RFC 3209, *RSVP-TE: Extensions to RSVP for LSP Tunnels*, defines the capabilities of extended RSVP” in a section entitled “Understanding RSVP-TE.” Ex. 5 at 148, 150. Based on the above, the Court should adopt Cisco’s construction.

#### **B. Preamble (claim 15)**

Corrigent appears to agree in principle that the preamble should be limiting with respect to “a first MPLS/LAG switch and a second MPLS/LAG switch.” Opp. at 30. Corrigent even agrees that this language “provides context for the invention in the claim body.” *Id.* This is precisely why the preamble should be limiting. Because Corrigent does not appear to dispute this portion of the preamble, Cisco focuses its reply on the remaining portions of the preamble, which recite “[a]n apparatus for assigning and utilizing an Ethernet physical data port in an Ethernet Link Aggregation Group (LAG) located downstream from a preceding node in a Multi-Protocol Label Switching (MPLS) network tunnel employing Resource Reservation Protocol Traffic Engineering

(RSVP-TE) tunnel provisioning.” ’602 patent, cl. 15.

LAG, MPLS and RSVP-TE are all necessary limitations on the claim scope. LAG, MPLS and RSVP-TE are fundamental to the operation of the alleged invention of the ’602 patent. In fact, the background of the invention incorporates by reference standards that pertain to MPLS (RFC 3031), RSVP-TE (RFC 2205 and RFC 3209) and LAG (IEEE 802.3ad). *See* ’602 patent at 1:25–2:17. While the body of the claim does not recite RSVP-TE, as Corrigent argues, the claim body still relies on the RSVP-TE tunneling provision recited in the preamble. The claim limitations directed to the “network tunnel” are in reference to the RSVP-TE tunneling provision as recited in the preamble. Further support for this may be found in the specification. According to the ’602 patent, RFC 2205, entitled “Resource ReSerVation (RSVP)—Version 1,” defines an “admission control” decision module. *See id.* at 1:50–60. “The admission control module is used in RSVP-TE for setting up *MPLS tunnels*.” *Id.* at 1:60–61 (emphasis added). Thus, these protocols are “necessary to give life, meaning, and vitality to the claim.” *Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002).

## V. CONCLUSION

For the reasons set forth in its Opening Brief, and those set forth herein, Cisco respectfully requests that this Court adopt Cisco’s constructions.

Respectfully submitted,

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By: */s/ Shaun W. Hassett, with permission  
by Brian A. Rosenthal*

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# **EXHIBIT 2A**

## **Curriculum Vitae of Dr. James L. Olivier**

### **PROFESSIONAL SUMMARY**

The foundation for my career began over thirty years ago with a Doctorate in Electrical Engineering.

I am currently a Research Professor at Southern Methodist University's Hunt Institute and Adjunct Professor in Network Engineering Program at SMU's Graduate School of Electrical and Computer Engineering. I am also the owner of Olivier Consulting, where I provide consulting services for advanced network / system design along with IP consulting. In addition, I am also a member of the technical staff of McAlexander Sound, where I specialize in Telecommunications Architecture / Computer Software. Recently I have been appointed Research Professor at SMU's Hunt Institute for Engineering and Humanity specializing in Transformational Technologies.

I have three degrees from The Ohio State University: a Bachelor of Science degree in Electrical Engineering; a Master of Science degree in in Electrical Engineering and a Doctor of Philosophy degree in Electrical Engineering. I have published papers in the areas of coding theory and multiprocessor computer systems.

Over the last 20 years I have devoted my attention to industry consulting in the areas of intellectual property and networking technologies.

### **EDUCATION PROFILE**

Ph.D. Electrical Engineering, The Ohio State University, Columbus, Ohio, 1988 Dissertation: "*Concurrent Error Detection in Arithmetic Processors using GAN Codes*", Received separate minors in fields of Computer Science, Microelectronics and Semiconductor Fabrication, and Discrete Mathematics.

Recipient of the prestigious Kodak Fellowship, awarded nationally to 12 doctoral students in the fields of science and engineering.

MS. Electrical Engineering, The Ohio State University, Columbus, Ohio, 1985 Thesis: "*A Navigation System for a Vehicle with a Laser Rangefinder*"; Major areas of study were robotics and artificial intelligence.

## **Curriculum Vitae of Dr. James L. Olivier**

BS. Electrical Engineering, The Ohio State University, Columbus, Ohio, 1983 Cum Laude.

### **EXPERIENCE PROFILE**

2022 – present     **Research Professor at SMU's Hunt Institute for Engineering and Humanity Southern Methodist University**

- Program Lead of Hunt Institute's Transformational Technology Hub responsible for strategy formulation and project implementation.

2019 – 2022     **Program Lead and Adjunct Executive in Residence SMU's Hunt Institute for Engineering and Humanity Southern Methodist University**

- Program Lead of Hunt Institute's Transformational Technology Hub responsible for strategy formulation and project implementation.

2017 - present     **Adjunct Professor for Network Engineering Program at Southern Methodist University's Lyle School of Electrical Engineering**

- Teaching Advanced Switching and Routing with MPLS at SMU's nationally rated Telecommunications and Network Engineering program. Research interests include SDNs, Video Transport, SD-WANs, Blockchain, IoT, and In-Networking Processing.

2003 - present     **Olivier Consulting – Dallas Texas  
IP Consultant M<sup>c</sup>Alexander Sound**

- Technology Research and Intellectual Property Management, including, IP Protection, IP Validity, IP Portfolio Valuation, IP Strategy and IP Technical Consultation. Clients include Arista Networks, HTC Corporation, T-Mobile, Samsung, Vizio, Google Corporation, Level 3 Communications, AT&T, Amazon, Ericsson, and S.T Microelectronics.

Recognized Expert before United States Federal District Courts in the Areas of

- Congestion Control in Packet Switching  
*QPSX v Nortel 2:05-CV-268, 2007*

## Curriculum Vitae of Dr. James L. Olivier

- Cellular High Speed Packet Access Networks  
*Wi-LAN Inc., v. Alcatel-Lucent et. al CV-6:10, 2013*
- Signaling Protocols in Cellular Networks  
*Core Wireless Licensing S.A.R.L v. Apple 6:12-CV-100, 2015*

Recognized Expert before the International Trade Commission in the Areas of

- Security and Firewalls in Routers and Switches;  
*Investigation 337-TA-628, 2007*
- Cellphone Hardware and Software for Imaging;  
*Investigation 337-TA-726, 2010*
- Operating Systems for Mobile Devices;  
*Investigation 337-TA-744, 2011*
- Mobile Devices Hardware and Software Architectures;  
*Investigation 337-TA-850, 2012*
- Ethernet Switch Packet Processor Hardware and Software;  
*Investigation 337-TA-945, 2015*

Lead Technology Research and Intellectual Property investigations in the following areas

- Technology related to mobile camera system's software systems architecture. *HTC Corporation*
- Technology related to gateway protocols between Cellular /PSTN Networks and the Internet. Investigated the design of a Packet Gateway and associated soft switch. *Level 3 Communications*
- Technology related to content delivery server systems based on demographic information received from client systems. *AT&T*
- Technology investigation related to Metro Ethernet, MPLS, 802.17, and 802.3 access products. *Transpacific IP*
- Technology investigation related to the research, specification, design, and architecture of the Telstrat's Next Generation Switch, which provided video, including analog, digital, HDTV, along with IP based voice, and also provided internet service. *Telstrat*

## **Curriculum Vitae of Dr. James L. Olivier**

- Technology investigation into the specification, design, and architecture of the Crane Wireless Sensor Network. Investigated scalability, address assignment, access, and security for a large IoT Wireless Sensor Network. *Crane Aerospace*

2002 - 2003  
**Manager**

### **Navini Networks - Richardson, Texas Senior**

- Performed research and development in Navini's Wireless CDMA broadband System. Responsible for definition and implementation of layer 2 and layer 3 network protocols for Navini's Broadband Wireless Products. Developed servers for network security, network services, service provisioning and subscriber management for a CDMA network. Responsible for the design and development of a sign-on web site which managed and authorized users for different services in a broadband CDMA network. This system consisted of multiple Apache Web Servers providing the web pages to the users and a centralized key storage facility to manage the various keys needed to authorize the different services.

1999 – 2002

### **Marconi Communications - Irving, Texas Manager of Systems Engineering**

- Responsible for design and development of new products and product evolution for Marconi's North American Access Division. I developed systems for the access video market, such as Digital Subscriber Line (DSL) networks, Hybrid fiber-coaxial (HFC) networks and DOCSIS systems. These systems were triple play systems which provide voice, video and data. While at Marconi, I was also responsible for the web servers design for the Network Management System for the North American Access product division.

1996– 1999

### **Samsung Telecommunications America - Richardson, Texas Principal Engineer**

- Responsible for Service Control subsystem of Samsung's next generation wireless broadband UMTS switching system. Designed and developed a Java based platform for defining services for Samsung's next generation high-speed wireless switch. Areas of responsibility include traditional telephony services, wireless services, broadband

## **Curriculum Vitae of Dr. James L. Olivier**

services, and Internet services, such as an email portal. While at Samsung, I was also their corporate representative to the International Telecommunication Union, ("ITU"), which is the agency of the United Nations responsible for information and communication technologies. I was also Samsung's corporate representative to the 3GPP standards body. It was there that I participated in the development of standards for advanced wireless networks, including multimedia transport.

**1995 – 1996                      DSC Communications Switch Products Division –  
Plano, Texas**

### **Senior Manager: Intelligent Network Evolution and Business Planning**

- Responsible for architecture and development of DSC's Intelligent Network product line. These products demonstrated at SuperComm 1996; a U.S. telecommunications trade show showed the integration of streaming media servers together with the interactivity of the Internet. I also actively interacted with key customers on their system designs and participated in relevant standards work.

### **Senior Manager: ATM Systems Engineering Group**

- Lead the systems engineering group in defining a new high-speed ATM switches for enterprise and telecommunication networks. These efforts include, multiprocessor architectures, communications subsystems, and software architectures. In addition, I was responsible for responding to RFIs and RFPs for a number of clients server based multimedia systems and served as DSC corporate representative to the ATM Forum.

**1990 – 1995                      AT&T Bell Laboratories - Columbus, Ohio  
Member of Technical Staff**

- Designed and implemented a variety of multiprocessor systems for use in the computer/multimedia systems. These systems included Asynchronous Transfer Mode 'ATM' based Internet and video distribution system. I also participated in the design and development of client server based systems for database access. At this time, I also began my work with standard settings bodies. While at AT&T Bell Laboratories in 1990s, I was charged with monitoring standard setting bodies such as the ATM Forum and DAVIC, the Digital Audio-Visual Council.

## **Curriculum Vitae of Dr. James L. Olivier**

1989 – 1990            **General Motors Research Laboratories Warren  
Michigan**

**Senior Research Engineer: Computer Science  
Department**

- Conducted research into basic computer science problems associated with the future development of vehicular systems. These areas include the design of fault tolerant control systems, new cost affective microprocessor architectures and software for reliability and performance modeling. Lead the development of an automotive testbed for the evaluation of prototype systems.

1988 – 1989   **Harris Communications – Melbourne, Florida  
Principal Engineer**

- Conducted research and development into innovative computer systems for use in space systems. Studied coherency protocols for microprocessor memory systems. Developed fault tolerant multi-processor computer systems for use in Strategic Defense Initiative.

### **PUBLICATIONS**

Olivier, J., Ozguner, F. “*A navigation algorithm for an intelligent vehicle with a laser rangefinder*”, Proceedings of the 1986 IEEE International Conference on Robotics and Automation, Vol. 3, April 1986.

Olivier, J. L. and Ozguner, F. “*Design of Concurrent Error Detecting Systolic Arrays Using GAN Codes*” IEEE Transactions on Computer Aided Design, vol. 9, no. 10 October 1989.

Olivier, J.L. “*Low Cost Residue Prediction for Improved Addition Efficiency*”, G. M. Research Publication, December 1989.

Olivier, J.L. and Tkacik, T.E., “*RELY, a Markov Modeling Package for System Reliability Prediction*” G.M. Research Publication, January 1990.

### **ISSUED PATENTS AND PATENT APPLICATIONS**

## **Curriculum Vitae of Dr. James L. Olivier**

- US 8334775 RFID-based asset security and tracking system, apparatus and method Network based asset management system.
- US 20090174772 Security and surveillance system Network based surveillance and security system.
- US 20130201337 Rfid-based asset security and tracking system, apparatus and method Network based asset management system.

### **ADDITIONAL ACTIVITIES**

Member of the Social Enterprise Advisory Council at the Hunt Institute for Engineering & Humanity, which is a member of the United Nations Sustainable Development Solutions Network.

Fellow at SMU's Hunt Institute for Engineering and Humanity.

Chairman of IEEE Dallas Blockchain Group

## Cases Worked Past 5 Years

### Year Engaged

#### 2022

Expert Engagement: Licensing  
Type of Matter: Consulting  
Case Name:  
Engaged on behalf of: Ericsson  
Technology at Issue: Power Control in Cellular Networks  
Services Provided: Consulting  
Law Firm: BakerBotts  
Year Engaged: 2022

Expert Engagement: Litigation  
Type of Matter: Provide Opinion  
Case Name: Telecom Network Solutions, LLC v. T-Mobile USA, Case No. 2:21-cv-00418-JRG  
Engaged on behalf of: T-Mobile and Sprint Spectrum  
Technology at Issue: QoS in Cellular Networks  
Services Provided: Consulting  
Law Firm: K&L Gates LLP  
Year Engaged: 2022

Expert Engagement: IPR  
Type of Matter: Inter partes review  
Case Name: PTAB IPR on U.S. Patent No. 7,623,033 and 8,766,797  
Engaged on behalf of: Qualcomm  
Technology at Issue: Sensor networks  
Services Provided: Wrote Declarations  
Law Firm: Norton Rose  
Year Engaged: 2022

## Curriculum Vitae of Dr. James L. Olivier

Expert Engagement: Litigation  
Type of Matter: Inter partes review  
Case Name: PTAB IPR on  
U.S. Patent No. 10,325,159  
Engaged on behalf of: Vivint  
Technology at Issue: Electronic Monitoring  
Services Provided: Wrote Declarations  
Law Firm: Foley and Lardner  
Year Engaged: 2022

Expert Engagement: Patent Review  
Type of Matter: Inter partes review  
Case Name: PTAB IPR on  
U.S. Patents No. 9,965,233, 9,389,822  
Engaged on behalf of: Roku, Inc.  
Technology at Issue: Protected or Encrypted Content delivery over Internet  
Services Provided: Wrote Declarations  
Law Firm: Perkins Coie  
Year Engaged: 2022

Expert Engagement: Litigation  
Type of Matter: Expert Consulting  
Case Name: Corrigent Corporation v. Cisco Systems, Dell and Arista  
Networks 6:22-cv-00396-ADA-DTG, 1:22-cv-00496-RGA,  
22-497-RGA  
Engaged on behalf of: Corrigent Corporation.  
Technology at Issue: 3GPP Network Elements  
Services Provided: Wrote Declarations  
Law Firm: Steptoe & Johnson  
Year Engaged: 2022

## **2021**

Expert Engagement: Litigation

## Curriculum Vitae of Dr. James L. Olivier

Type of Matter: Inter partes review  
Case Name: PTAB IPRs on  
U.S. Patent No. 7,979,070, 8,879,503  
Engaged on behalf of: Thales AIS DIS  
Technology at Issue: Signaling Messages in 3GPP networks  
Services Provided: Wrote Declaration  
Law Firm: AddyHart LLP  
Year Engaged: 2021

Expert Engagement: Litigation  
Type of Matter: Inter partes review  
Case Name: PTAB IPR on  
U.S. Patent No. 10,346,114  
Engaged on behalf of: Roku, Inc.  
Technology at Issue: Content delivery over wireless networks  
Services Provided: Wrote Declarations  
Law Firm: Perkins Coie  
Year Engaged: 2021

Expert Engagement: Litigation  
Type of Matter: Inter partes review  
Case Name: PTAB IPR on  
U.S. Patent No. 7,580,388  
Engaged on behalf of: Thales AIS DIS  
Technology at Issue: Signaling Messages in 3GPP networks  
Services Provided: Wrote Declarations  
Law Firm: AddyHart LLP  
Year Engaged: 2021

Expert Engagement: PTAB  
Type of Matter: Inter partes review  
Case Name: PTAB IPR on  
U.S. Patent No. 9,54,426, 10,924,500, and 9,372,098  
Engaged on behalf of: Ericsson Inc.  
Technology at Issue: Signaling Messages in 3GPP networks

## Curriculum Vitae of Dr. James L. Olivier

Services Provided: Wrote Declaration, Deposition Testimony  
Law Firm: Baker Botts  
Year Engaged: 2021

Expert Engagement: PTAB  
Type of Matter: Inter partes review  
Case Name: PTAB IPRs or PGR on  
U.S. Patent No. 10,601,948, 11,190,622, 11,206,317,  
11,272,034, 11,349,953, 11,616,826, 10,965,770  
Engaged on behalf of: Metacluster  
Technology at Issue: Computer networks  
Services Provided: Wrote Declarations, attended depositions  
Law Firm: Norton Rose  
Year Engaged: 2021

### **2020**

Expert Engagement: Litigation  
Type of Matter: Patent  
Case Name: Intellectual Ventures I LLC and Intellectual Ventures II LLC  
v. VMware, Inc., Western District of Texas Case No. 6:19-  
cv-449  
Engaged on behalf of: VMware  
Technology at Issue: Layer 3 Networking  
Services Provided: Wrote Declaration  
Law Firm: Winston & Strawn  
Year Engaged: 2020

Expert Engagement: Litigation  
Type of Matter: Patent  
Case Name: Exafer Ltd. v. Microsoft Corporation, Case No: 20-CV-  
00131 ADA  
Engaged on behalf of: Microsoft  
Technology at Issue: Layer 2 forwarding in Data Center

## Curriculum Vitae of Dr. James L. Olivier

Services Provided: Wrote Declarations, attended depositions  
Law Firm: Winston & Strawn  
Year Engaged: 2020

Expert Engagement: Litigation  
Type of Matter: Copyright  
Case Name: Apple Inc. v Corellium, LLC  
CASE NO. 9:19-cv-81160-rs Southern District of Florida  
Engaged on behalf of: Corellium LLC  
Technology at Issue: Software and image copyrights  
Services Provided: Wrote Declaration, attended deposition  
Law Firm: Hecht Partners LLP  
Year Engaged: 2020

Expert Engagement: Litigation  
Type of Matter: Inter partes review  
Case Name: PTAB IPR on  
U.S. Patent No. 7,894,443  
Engaged on behalf of: Thales AIS DIS  
Technology at Issue: Radio Link Control  
Services Provided: Wrote Declaration  
Law Firm: AddyHart LLP  
Year Engaged: 2020

Expert Engagement: Litigation  
Type of Matter: Inter partes review  
Case Name: Sisvel International S.A. and 3G Licensing S.A. v.  
Cradlepoint, Inc., Case No. 1:19- CV-1142-MN (District of  
Delaware)  
Engaged on behalf of: Cradlepoint and Sierra Wireless  
Technology at Issue: Radio Link Control  
Services Provided: Wrote Declaration  
Law Firm: Perkins Coie  
Year Engaged: 2020

## Curriculum Vitae of Dr. James L. Olivier

Expert Engagement: PTAB Case No. IPR2021-00260  
Type of Matter: Inter partes review  
Case Name: PTAB IPR on U.S. Patent No. 9, 723,813 to Davis  
Engaged on behalf of: Tomofun  
Technology at Issue: Animal Interaction System  
Services Provided: Wrote Declaration  
Law Firm: Greenberg Traurig, LLP  
Year Engaged: 2020

### **2019**

Expert Engagement: Litigation  
Type of Matter: Patent Investigation  
Case Name: SIMO Holdings v Hong Kong uCloudlink Networks Technology Limited and uCloudlink (America) LTD.  
CASE NO. 1:18-cv-05427 Southern District NY  
Engaged on behalf of: uCloudlink Ltd  
Technology at Issue: Wireless data links  
Services Provided: Wrote Declarations  
Law Firm: Fish & Richardson

Year Engaged: 2019

Expert Engagement: Litigation  
Type of Matter: Patent Investigation  
Case Name: Harris Corporation v. Huawei Device USA, Inc., et al.  
Case No. 2:18-cv-439 ED-TX  
Engaged on behalf of: Huawei Device USA  
Technology at Issue: Network Security  
Services Provided: Wrote Declaration, Gave Deposition testimony  
Law Firm: Ropes & Gray LLP  
Year Engaged: 2019

Expert Engagement: Consulting  
Type of Matter: Consulting  
Case Name:  
Engaged on behalf of: Photobucket

## Curriculum Vitae of Dr. James L. Olivier

Technology at Issue: Photo distribution in wireless networks  
Services Provided: Analysis of content distribution in wireless networks  
Law Firm: Norton Rose  
Year Engaged: 2019

Expert Engagement: Consulting  
Type of Matter: Opinion regarding U.S. Pat. Application 2014/0192800,  
Case Name:  
Engaged on behalf of: SonicTube Research  
Technology at Issue: Packetized wireless networks  
Services Provided: Declaration  
Law Firm: SonicTube Research  
Year Engaged: 2019

## **2018**

Expert Engagement: Inter Partes Review  
Type of Matter: Patent Review  
Case Number: IPR2017-00829, -00830, -01131, -01133  
Engaged on behalf of: Vidstream LLC  
Technology at Issue: Networked Video  
Services Provided: Wrote Declaration, attended deposition  
Law Firm: Norton Rose  
Year Engaged: 2018

Expert Engagement: Litigation  
Type of Matter: Patent Investigation  
Case Name: Arista Networks, Inc. v. Cisco Systems, Inc. No. 5:16-CV-00923-BLF (N.D. Cal.)  
Engaged on behalf of: Arista Networks  
Technology at Issue: Network protocols  
Services Provided: Signed Declaration  
Law Firm: Tensegrity Law Group  
Year Engaged: 2018

## Curriculum Vitae of Dr. James L. Olivier

Expert Engagement:	Litigation
Type of Matter:	Patent Investigation
Case Name:	Intellectual Ventures I LLC v. HCC Insurance Holdings Inc. CA No. 6:15-cv-00660 ED-TX
Engaged on behalf of:	HCC Insurance Holdings
Technology at Issue:	Back end web site technology
Services Provided:	Wrote expert report, attended deposition
Law Firm:	Norton Rose Fulbright
Disposition:	Settled
Year Engaged:	2018

### **2017**

Expert Engagement:	Inter Partes Review
Type of Matter:	Patent Review
Case Number:	IPR2018-00287
Engaged on behalf of:	Comtech Mobile Datacom Corporation
Technology at Issue:	Vehicle Mapping Technology
Services Provided:	Wrote Declaration
Law Firm:	Perkins Coie LLP
Year Engaged:	2017

Expert Engagement:	ITC Matter
Type of Matter:	Patent Investigation
Case Name:	ITC Inv.No.337-TA-1057 Certain Robotic Vacuum Cleaning Devices and Components Thereof Such as Spare Parts,
Engaged on behalf of:	Shenzhen Silver Star Intelligent Technology
Technology at Issue:	Autonomous Vehicle Technology
Services Provided:	Wrote expert report, gave deposition and hearing testimony
Law Firm:	Pillsbury Winthrop Shaw Pittman
Year Engaged:	2017

## Curriculum Vitae of Dr. James L. Olivier

### **2016**

Expert Engagement: Litigation and Inter Partes Review  
Type of Matter: Patent Investigation  
Case Name: International Business Machines Corp. v. The Priceline Group Inc., et al C.A. No. 15-137-LPS, and IPR2016-00608 and IPR2016-00609.  
Engaged on behalf of: The Priceline Group Inc.  
Technology at Issue: Web site Technology  
Services Provided: Wrote Expert Reports on Invalidity and Non-infringement. Attended Deposition.  
Law Firm: Norton Rose Fulbright  
Year Engaged: 2016

Expert Engagement: Litigation  
Type of Matter: Patent Investigation  
Case Name: Evolv, LLC v. Joyetech USA, Inc.  
Case No. 8:16-cv-00459-CJC-JCG CD-CA  
Engaged on behalf of: Joytech USA  
Technology at Issue: Computer controlled voltage source  
Services Provided: Wrote Declaration  
Law Firm: Pillsbury Winthrop Shaw Pittman LLP  
Disposition: Settled  
Year Engaged: 2016

Expert Engagement: Inter Partes Review  
Type of Matter: Patent Review  
Case Number: IPR2016-01431  
Engaged on behalf of: HCC Insurance Holdings  
Technology at Issue: Web site design; Network Agent Technology  
Services Provided: Wrote Declarations for IPR  
Law Firm: Norton Rose Fulbright  
Disposition: Settled  
Year Engaged: 2016

# **EXHIBIT 2B**



US005420985A

**United States Patent** [19]

Cantrell et al.

[11] Patent Number: **5,420,985**[45] Date of Patent: **May 30, 1995**

[54] **BUS ARBITER SYSTEM AND METHOD  
UTILIZING HARDWARE AND SOFTWARE  
WHICH IS CAPABLE OF OPERATION IN  
DISTRIBUTED MODE OR CENTRAL MODE**

[75] Inventors: **Jay Cantrell, Dallas; Ed Schurig,  
Plano, both of Tex.**

[73] Assignee: **Texas Instruments Inc., Dallas, Tex.**

[21] Appl. No.: **921,189**

[22] Filed: **Jul. 28, 1992**

[51] Int. Cl.<sup>6</sup> ..... **G06F 13/36**

[52] U.S. Cl. .... **395/325; 370/85.2;  
364/242.6; 364/242.92; 364/240; 364/240.2;  
364/DIG. 1; 364/232.9**

[58] Field of Search ..... **395/325, 725, 425;  
340/825.5; 370/85.2, 85.6**

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

4,402,040	8/1983	Evelt	364/200
4,766,536	8/1988	Wilson, Jr. et al.	364/200
4,779,089	10/1988	Theus	340/825.5
4,787,033	11/1988	Bomba et al.	364/200
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4,980,854	12/1990	Donaldson et al.	364/900
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5,253,348 10/1993 Scalise ..... 395/325  
5,261,109 11/1993 Cadambi et al. .... 395/725

*Primary Examiner*—Gopal C. Ray

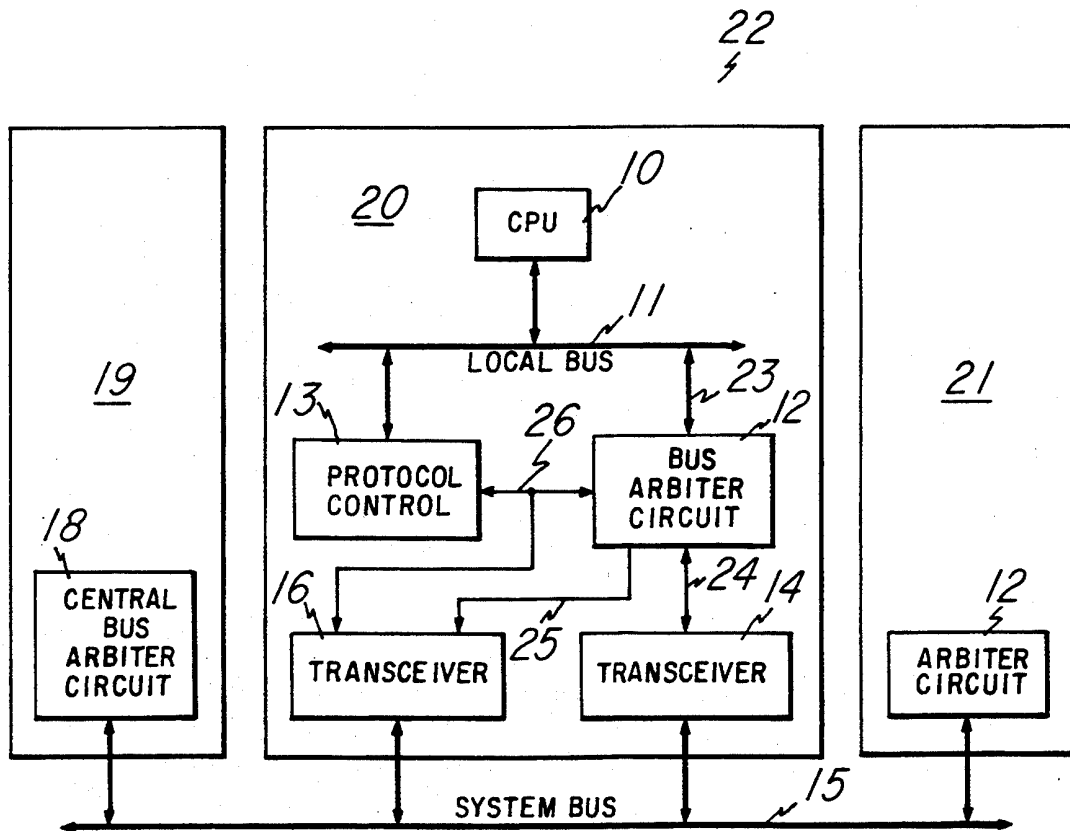
*Attorney, Agent, or Firm*—Rose Alyssa Keagy; Richard  
L. Donaldson

[57]

**ABSTRACT**

A system module 20 includes a processor 10, a system bus 15, a local bus 11 coupled to the processor, arbitration circuitry 12 coupled to the local bus and the system bus for providing common hardware protocol for distributed mode and central mode operations, and protocol control circuitry 13 coupled to the arbitration circuitry, the system bus, and the local bus for providing a system bus request to the arbitration circuitry when the system module desires to perform a bus transaction. The local bus 11 may be a processor bus on a system module while the system bus 15 may be an architecture bus standard such as Futurebus+. Also a method of operating arbiter circuitry in distributed mode or central mode where no change in hardware or software is needed when switching system operations between distributed and central modes.

**30 Claims, 6 Drawing Sheets**



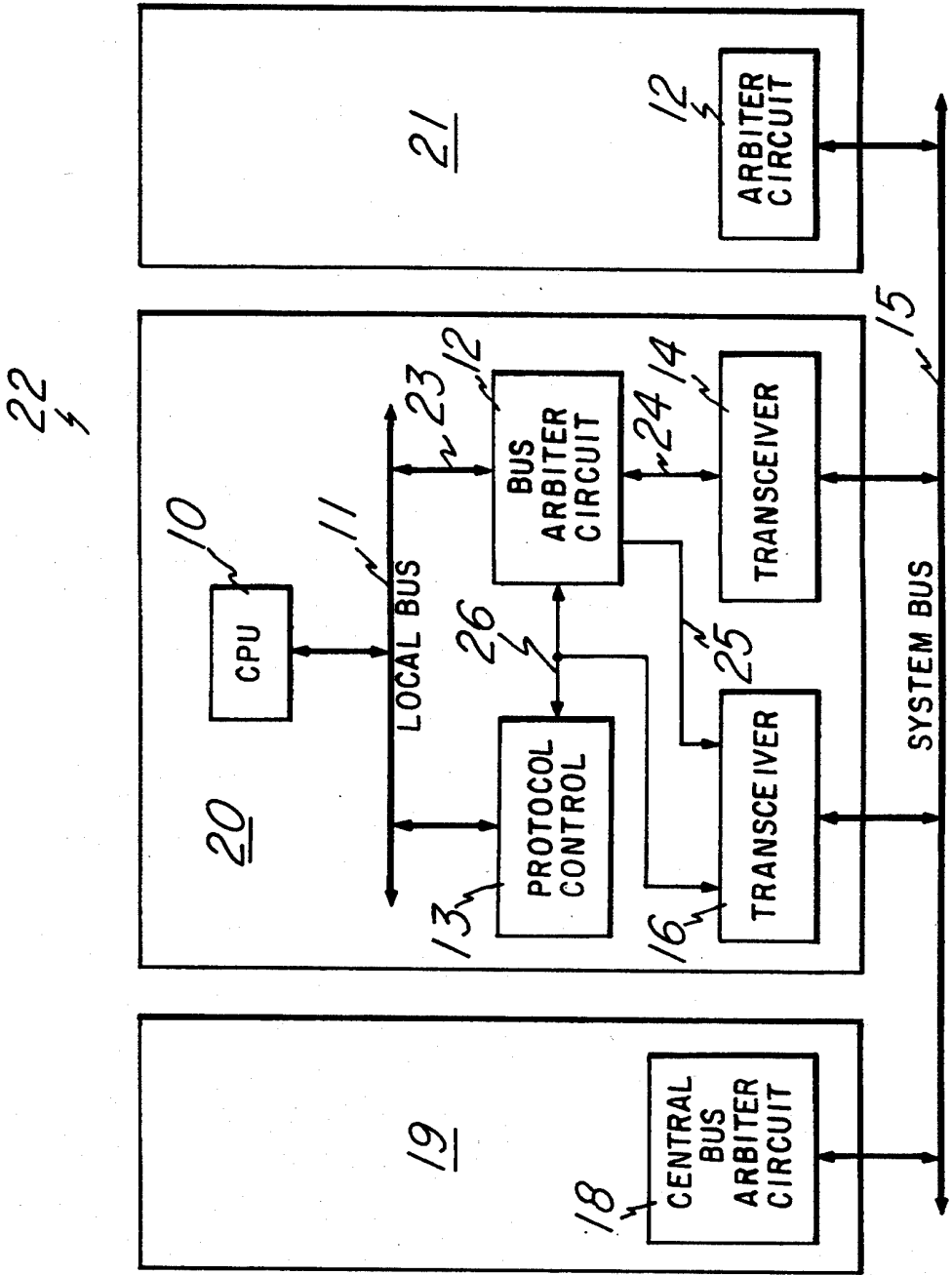


Fig. 1

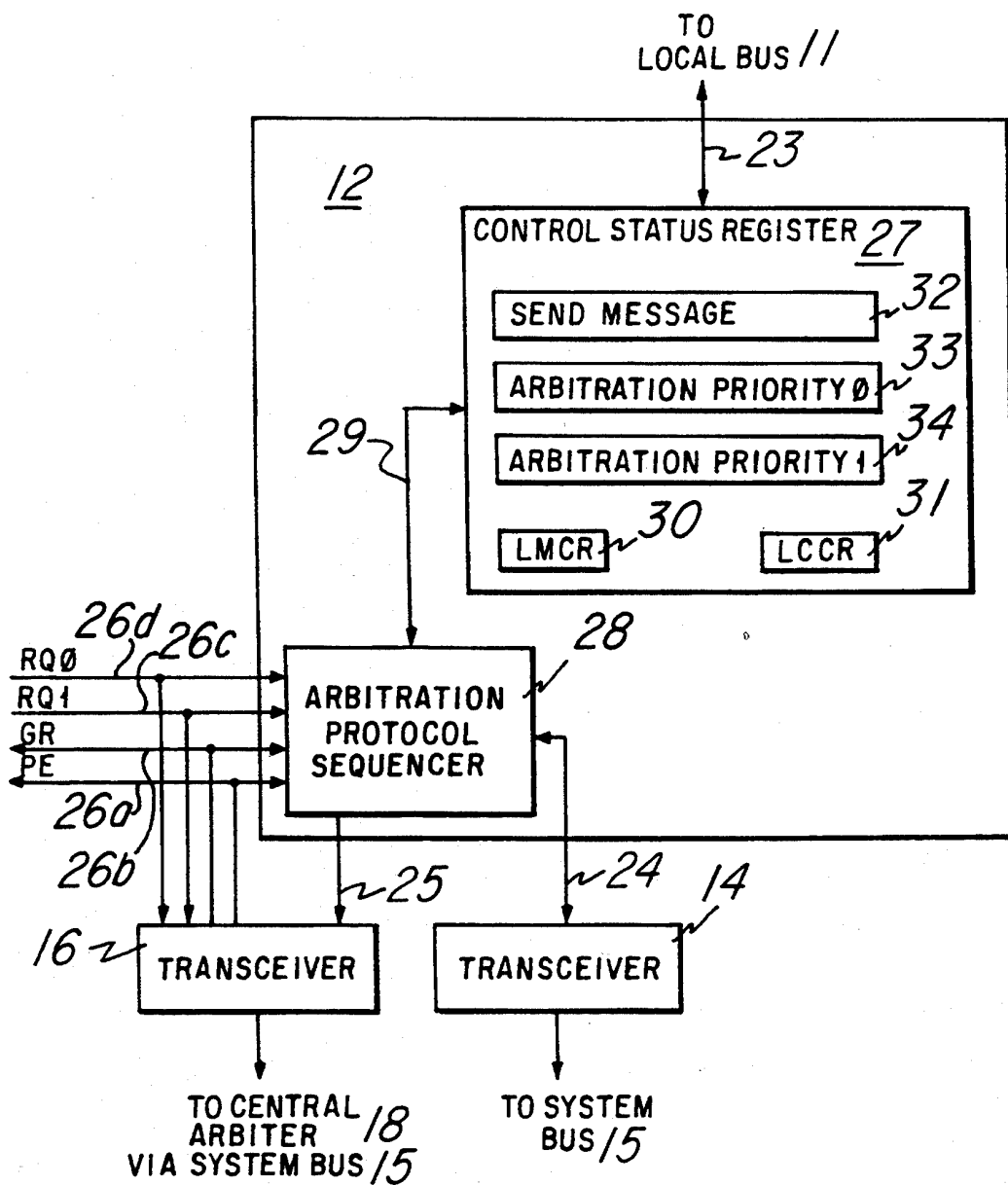
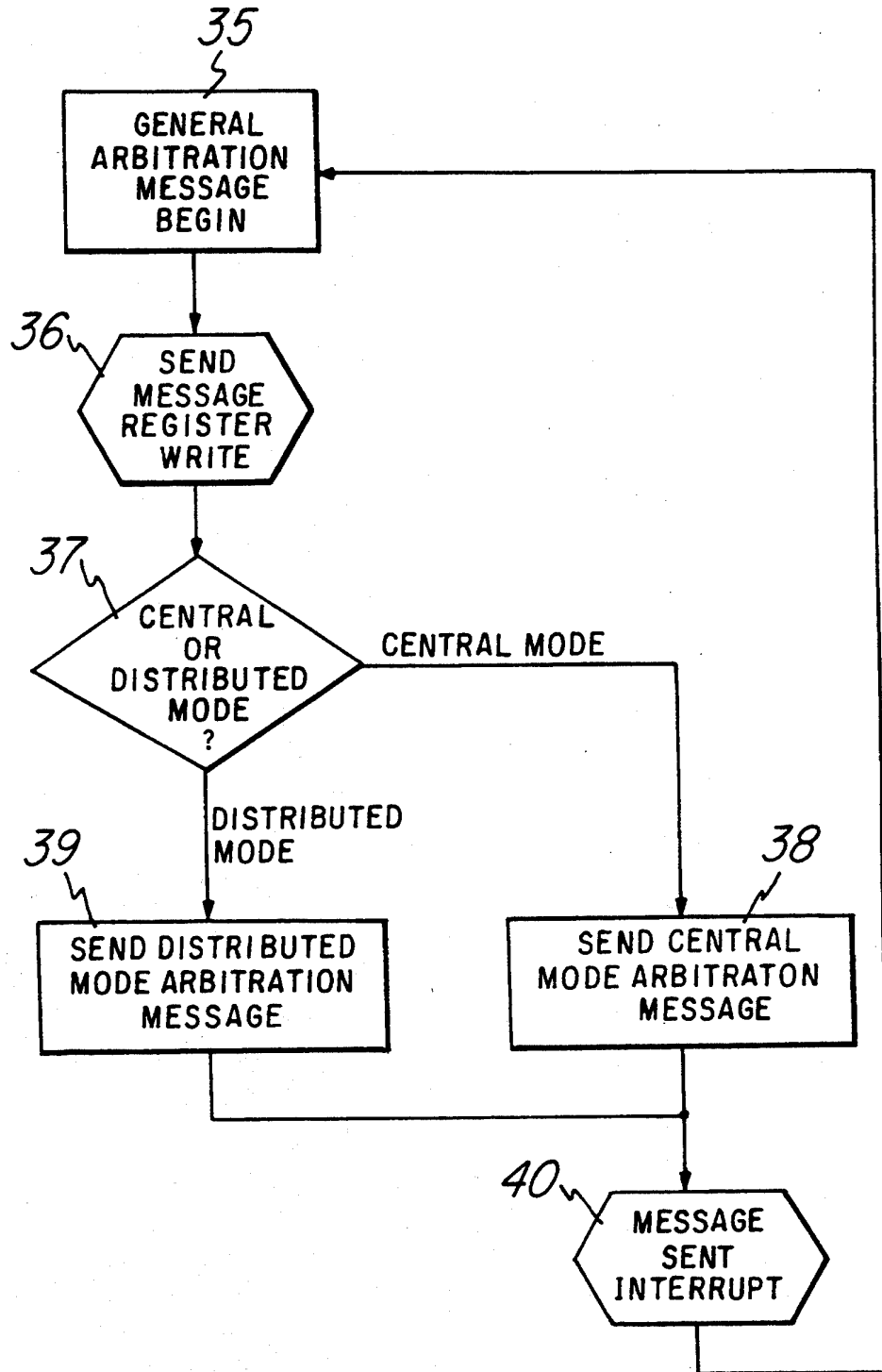


Fig. 2

*Fig. 3*

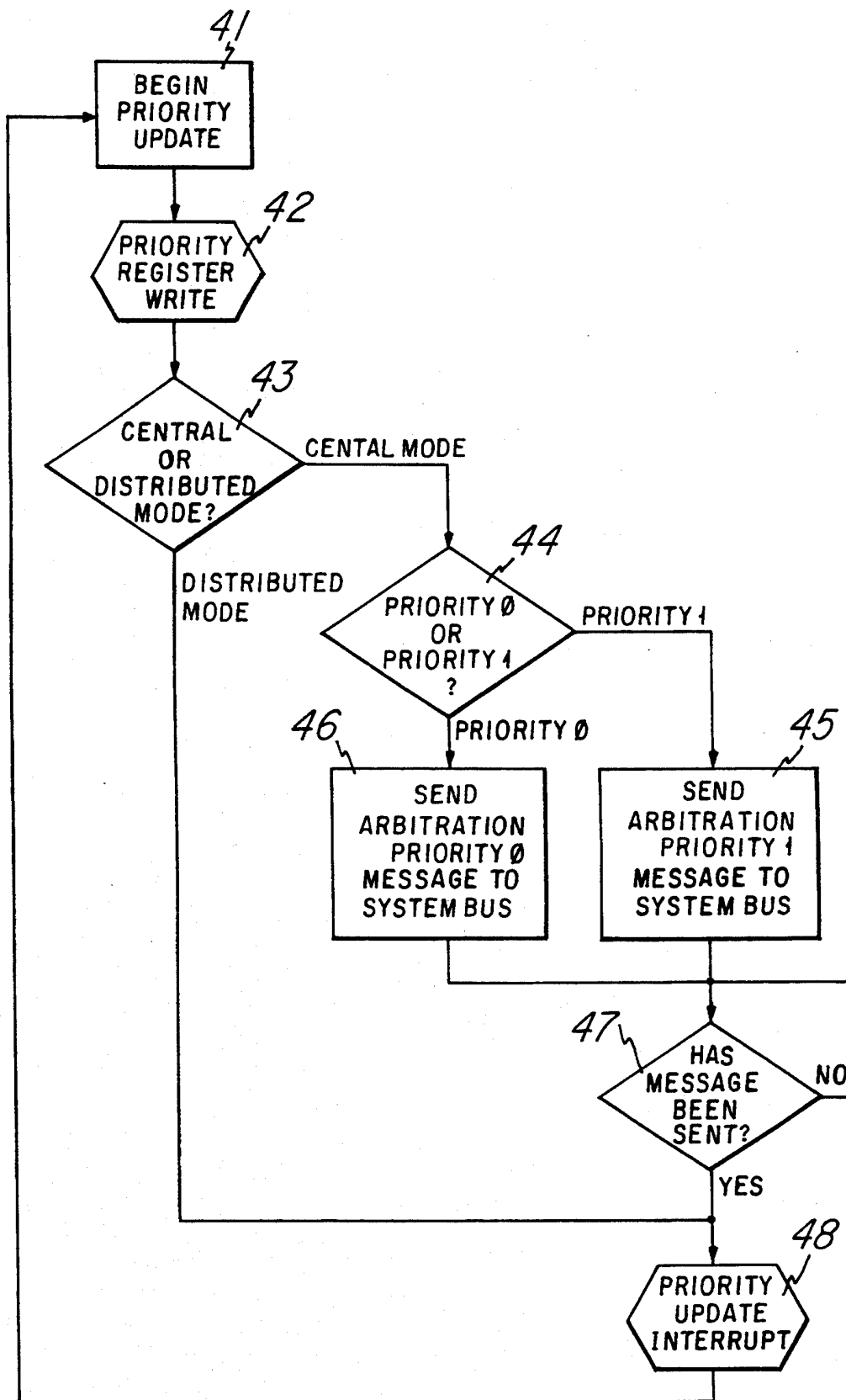


Fig. 4

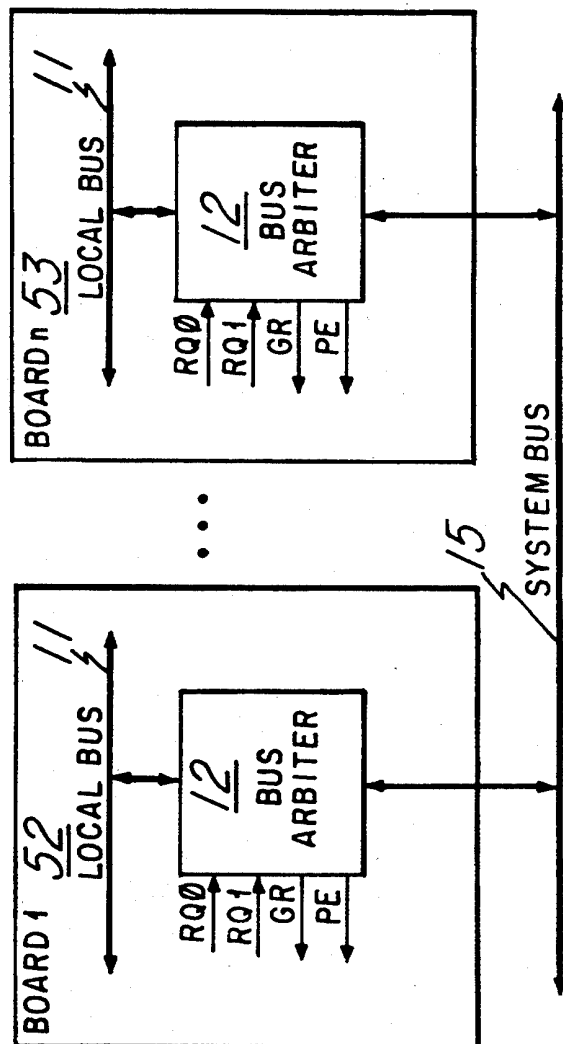
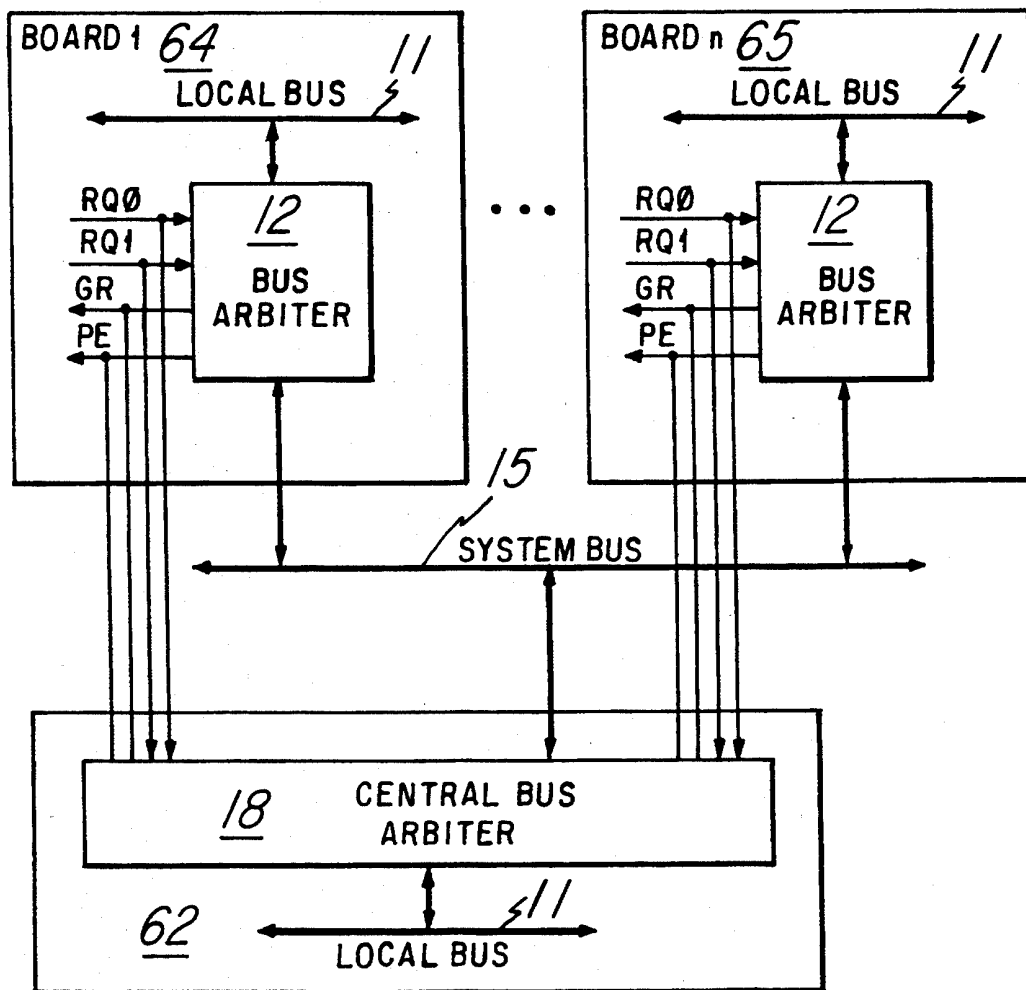


Fig. 5



*Fig. 6*

# **BUS ARBITER SYSTEM AND METHOD UTILIZING HARDWARE AND SOFTWARE WHICH IS CAPABLE OF OPERATION IN DISTRIBUTED MODE OR CENTRAL MODE**

## **FIELD OF THE INVENTION**

This invention relates generally to computers and specifically relates to bus system arbiter circuitry and methods.

## **BACKGROUND**

Futurebus+ is an IEEE specification for high-performance backplane-based computing that permits architectural consistency across a broad range of computer products. Key attributes of Futurebus+ are discussed in the article of J. Theus in *Microprocessor Report*, Volume 6, Number 7, May 27, 1992. Futurebus+ is a comprehensive architectural specification designed as an open standard; that is, an interface standard for which there are no preconceived restrictions in terms of architecture, microprocessor, and software implementations. It is also a standard explicitly designed to support multiple generations of computer technology, leading to system speeds significantly greater than current systems.

Futurebus+ provides a 64-bit architecture with a compatible 32-bit subset and data path extensions to 128 or 256 bits. The protocols, while providing headroom for system growth, explicitly support real-time scheduling, fault tolerance, and high-availability and high-reliability systems.

The logical layering of the Futurebus+ specifications offers a wealth of architectural features with which designers may implement a wide variety of systems. Both loosely coupled and tightly coupled compute paradigms are supported via the parallel protocols and in the message-passing and cache-coherence protocols. The control and status registers provide a standard software interface to the Futurebus+, easing the development and transportability of I/O drivers and other system software.

Unlike older standard buses, Futurebus+ is optimized for a backplane environment. Backplane transceiver logic (BTL) circuits provide incident-wave switching capability (thus no set up and hold times), low capacitance with high current drive capability, and controlled one-volt voltage swings for better noise margins.

Bus arbitration is the process of unambiguously issuing a single bus grant. Futurebus+ specifies doing bus arbitration through the use of either a central system or a distributed system.

The central system requires each module's arbitration circuitry to send a non-bused request and grant signal to the central arbiter.

The distributed system relies on bused signals to implement a distributed, asynchronous state machine and therefore does not use central facilities. The redundancy of distributed arbitration elements allows greater fault-tolerant operation. The distributed system is logically complex and significantly slower than the central system. The distributed system uses a byte-wide data path to choose a winner during the competition phase. This data path can also be used as a message facility that is completely independent of the main bus so it is useful for fault recovery and for signaling events.

Current arbitration systems require separate software and protocol hardware for central and distributed arbi-

tration modes. Such systems impose significant software and hardware overheads for fault tolerant systems.

It is a technical advantage of this invention to provide common run time software and common hardware protocol for distributed mode and central mode operations.

Other advantages of the invention will become apparent to those of ordinary skill in the art having reference to the following specification together with the drawings herein.

## **SUMMARY**

An arbitration circuit providing common hardware protocol for distributed mode and central mode operations. The arbitration circuit is coupled between a local bus, a system bus, and a protocol control circuit which provides a system bus request to the arbitration circuit when a system module desires to perform a bus transaction.

Preferably, the arbitration circuit further comprises common run time software for distributed mode and central mode operations. Transceivers are coupled to the arbitration circuit and the protocol control circuit for changing output signals from the arbitration circuitry to Backplane Transistor Logic (BTL) format used by the system bus and for allowing said output signals to be input onto the system bus. The arbitration circuit comprises an arbitration protocol sequencer coupled to the protocol control circuitry, register circuitry coupled to the arbitration protocol sequencer and the local bus, and a register for indicating whether the system is operating in central or distributed modes, making dynamic mode changes possible.

It is also preferable that the register circuit comprise a register for indicating whether or not the system module is master enabled, a register for storing an arbitration message, a plurality of registers for dynamically storing a plurality of priority levels, and registers storing the configuration, control, status, and test information needed for system bus arbitration. The system bus is preferably a Futurebus+.

This is also a method of switching arbiter circuitry from servicing a system module in central mode to distributed mode, comprising the steps of receiving a signal signifying that the system is in distributed mode, and imitating the signal protocol required by a system bus when communicating with a protocol control circuit.

Additionally, this is a method of operating arbiter circuitry in distributed mode comprising the steps of receiving service requests from a protocol control circuit, and performing distributed arbitration cycles to gain mastership of a system bus for a system module. Preferably, the method also includes the steps of sending arbitrated messages, receiving arbitrated messages, and storing arbitration messages in a register for access by a processor. No change in the hardware or software of the processor is needed when the system module switches operation between distributed mode and central mode.

Furthermore, this is a method of switching arbiter circuitry from servicing a system module in distributed mode to central mode, comprising the steps of receiving a signal signifying that the system is in central mode, and communicating with a protocol control circuit using the signal protocol required by a system bus.

Moreover, this is a method of operating arbiter circuitry in central mode comprising the steps of sending priority messages, enabling the appropriate transceivers to allow the central resource to grant and pre-empt the local module, wherein no hardware modification is needed when the system module switches operation between distributed mode and central mode. Preferably, no change in software of said processor is needed when the system module switches operation between distributed mode and central mode. Also the method preferably comprises the steps of sending arbitrated messages, receiving arbitrated messages, and storing received messages in a register for access by a processor.

This is also a method of performing a priority update in an arbiter circuit comprising the steps of writing to the priority register, determining whether system is in distributed or central mode, issuing an interrupt message if in distributed mode signifying that the priority is updated, determining which priority is to be updated if in central mode, sending the priority update message appropriate for the determined priority if in central mode, monitoring whether the message has been sent over system bus, and issuing the interrupt. Preferably no change in the hardware or software of the processor is needed when the system module switches operation between distributed mode and central mode.

Additionally, this is a method of sending a general arbitration message by an arbiter circuit comprising the steps of writing to a message register, determining whether system is in central mode or distributed mode, sending the message appropriate for central mode or distributed mode, issuing an interrupt message indicating said message has been sent, wherein no change in software of said processor is needed when the system module switches operation between distributed mode and central mode. Preferably, no hardware modification is needed when the system module switches operation between distributed mode and central mode.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a system incorporating the invention;

FIG. 2 is a logic diagram of the bus arbiter shown in FIG. 1;

FIG. 3 is a flow chart depicting a set of steps which may be used by the bus arbiter of FIG. 2 for sending a general message in accordance with the present invention;

FIG. 4 is a flow chart depicting a set of steps which may be used by the bus arbiter of FIG. 2 for performing a priority update in accordance with the present invention.

FIG. 5 is a block diagram showing a distributed mode only system configuration incorporating the invention.

FIG. 6 is a block diagram showing a programmable central arbiter system configuration incorporating the invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a block level diagram illustrating a computer system 22 within which the preferred embodiment of the invention operates. The computer system 22 includes a plurality of system modules 19, 20, 21 . . . n connected to a System Bus 15. System module 20 may contain a CPU 10 coupled to Local Bus 11. Also a Protocol Controller 13 and a Bus Arbiter Circuit 12 are

coupled to the Local Bus 11 and to each other. Protocol Controller 13 and Bus Arbiter Circuit 12 are also coupled to Transceivers 16 and 14. Transceivers 16 and 14 are coupled to System Bus 15.

The System Bus, 15, is preferably a Futurebus+. The system modules 19 . . . n may have a plurality of memory chips, CPUs, and/or peripheral (I/O) chips on them. The plurality of memory chips, CPUs, and I/O chips are able to communicate with one another via the System Bus 15. System module 20 may be a high-end computer board, performing a function such as, for example, regulating a flow system for the Space Shuttle.

CPU 10, for example, may comprise an Intel 486, or a Motorola 68040. While Local Bus 11, may comprise the buses that service a variety of microprocessors such as R4000, 680X0, 88XXX and 80X86. Transceivers 16 and 14 may comprise a SN74FB2031, SN74FB2032, or SN74FB2040, all manufactured by Texas Instruments. Protocol Control 13 and Bus Arbiter Circuit 12 may comprise common electrical components which together perform the function of autonomous control and arbitration for system bus and host module reads and writes known to those skilled in the art. This interface circuitry has been significantly improved by the addition of an improved Bus Arbiter Circuit 12.

The invention as shown in FIG. 2 contains the logic necessary to perform bus arbitration for systems operating in distributed mode or central mode with hardware and software that is mode independent.

FIG. 2 is a diagrammatic representation of a preferred embodiment of the Bus Arbiter 12 of FIG. 1. Control Status Register 27 is bidirectionally coupled to local bus 11 via Line 23. Arbitration Protocol Sequencer 28 is bidirectionally coupled to Register 27 via 29. Arbitration Protocol Sequencer 28 is also bidirectionally coupled to Protocol Control 13 and System Bus 15 via 26a-d.

Arbitration Protocol Sequencer 28 is also bidirectionally coupled to Transceiver 14 via 24 and Transceiver 16 via 25 and 26. Transceiver 16 is also bidirectionally coupled to Protocol Control 13 via 26.

Bus 24 is the main arbitration interface, performing the handshake between the Bus Arbiter 12 and System Bus 15. Bus 24 is used in both central and distributed mode to send messages to other bus agents, acquire the bus ownership in distributed mode, or in central mode to send priority updates to the central arbiter.

Line 23 provides register access, allowing the values in the registers of 27 to be loaded and observed. Within Control Status Register 27, Logical Module Control Register 30 indicates whether or not System Module 20 is master-enabled. This information is important when the system is operating in distributed mode. Logical Common Control Register 31 contains information indicating whether the system is operating in central mode or in distributed mode.

Send Message Register 32 contains the 8-bit arbitration message. When this register is written, an arbitration message is sent. Arbitration Priority Register 33 contains the 8-bit priority used when RQ0 (line 26d) is asserted. In distributed mode, this number is used to determine the arbitration number. In central mode, this number is used to automatically program the central arbiter via an arbitrated message. Arbitration Priority Register 34 contains the 8-bit priority used when RQ1 (line 26c) is asserted. In distributed mode, this number is used to determine the arbitration number. In central mode, this number is used to automatically program the

Central Arbiter 18 via an arbitrated message. Control Status Register 27 also contains other registers necessary for configuration, control, status and test applicable to arbitration.

In summary, Control Status Register 27 contains the Control Status Registers (CSR's) necessary to make Bus Arbitration Circuit 12 operate mode independent.

Signal 26a (PE) is the preempt signal which is driven high to indicate that a module with a higher priority has become the master-elect when the system is in distributed mode. This signal remains in the high impedance state while the system is in the central mode. Signal 26b (GR) is the grant signal used by Bus Arbiter 12 when the system is in distributed mode to indicate that system bus mastership has been granted. This signal remains in the high impedance state when the system is in central mode. Signals 26a and 26b (RQ0 and RQ1 respectfully) are the signal lines used by Protocol Control 13 to request system bus access.

Bus Arbiter 12 contains other circuitry capable of other functions, such as a filter that filters out unwanted messages, which are not essential to the understanding of this invention; therefore, they are not shown.

Bus Arbiter Circuit 12 provides for the use of common run time software and uses a common hardware protocol for distributed mode and central mode operations. Line 23 and Control Status Register 27 provide the capability for software independence. Line 26 and Arbitration Protocol Sequencer 28 provide the capability for hardware independence.

Referring again to FIG. 1, a detailed functional description of the common hardware protocol feature of the invention is provided.

In general, arbitration is trying to get access to a shared resource. The purpose of an arbiter is to gain mastership of the system bus for a particular electronic board such as system module 20. The board which gains mastership is the board with the highest priority.

Priority registers 33 and 34 shown in FIG. 2 contain the priorities that are being used by system module 20 to compete for mastership. These priorities can be dynamically changed by the CPU 10 between bus requests.

In central mode there is a Central Arbiter 18 that takes all of the requests from all the modules (20 . . . n) and determines which system module gains mastership. Then the Central Arbiter 18 sends a grant signal over the System Bus 15 to the system module who was awarded mastership. Therefore, the arbiter 12 in each module 20 . . . n is not involved in the arbitration process when the system is operating in central mode. In central mode the Central Arbiter 18 has to know each individual priority for each system module (i.e. 20 and 21) in order to determine which system module gains mastership of the System Bus 15. The Central Arbiter 18 obtains these priorities via arbitrated messages sent over the arbitration bus by each bus arbiter circuit 12.

In distributed mode each arbiter 12 on each module 20 . . . n is operating and following a system bus protocol to determine which system module gains mastership of System Bus 15. In distributed mode arbitration each system module's Bus Arbiter 12 receives the request signal from the system module's Protocol Control 13; obtains the priority out of the appropriate priority register (33 or 34) and then competes for access to the System Bus 15. Each system module's priority can be changed by CPU 10 via Line 23 between each system bus request. Thus, Bus Arbiter 12 has dynamic priority updating capability.

In distributed mode and in central mode the software writes the priority in either priority register 33 or 34. It is transparent to the software that in distributed mode the new priority was used by Bus Arbiter 12 but in central mode the new priority was sent over the System Bus 15 and then loaded to the Central Arbiter 18 for use by the Central Arbiter. For this reason the Bus Arbiter is software independent: to the software the writing of the priorities is identical whether the system is in central mode or in distributed mode.

The advantage of the invention is that Bus Arbiter Circuit 12 can be operated in either central mode or distributed mode without having to modify the hardware to operate in either of the two modes. This is because the same signals (RQ0, RQ1, GR, and PE) are used by Bus Arbiter 12 to talk to the protocol control 13 in both modes. The central mode handshake is imitated by the Bus Arbiter circuit 12 when the system is operating in distributed mode. Therefore, it is transparent to Protocol Control 13 whether Bus Arbiter Circuit is performing in central mode arbitration or distributed mode arbitration.

In summary, the distributed mode provides the same handshake as required for central mode, as dictated by the system bus specification. Thus, hardware independence is realized because there is a single interface between the arbitration circuitry and the protocol device.

Protocol Control 13 in FIG. 1 is responsible for the transfer of information over the System Bus 15. Protocol Control 13 sends a request via line 26 to the Bus Arbiter to gain access to the System Bus 15. Arbiter Circuit 12 interfaces to the arbitration portion of the System Bus 15. Once Bus Arbiter 12 gains access to the System Bus 15, Bus Arbiter 12 issues a Grant signal over line 26 allowing Protocol Control 13 to perform the needed data transfer. Once the data transfer is complete Protocol Control 13 releases the request on line 26 and Bus Arbiter releases the Grant over Line 26 thereby allowing another device or module to access the System Bus 15.

Referring now to FIG. 2, a further detailed description of the hardware interfaces for operating the Bus Arbiter 12 in distributed mode and central mode is provided.

Control signal 25 and bus 26 facilitate hardware independence for Bus Arbiter 12. In central mode control signal 25 is activated. When control signal 25 is activated controller output enables 26a and 26b are deactivated, and the transceiver outputs 26a and 26b are activated. Thus, PE and GR, 26a and 26b, are serviced by the central arbiter.

In distributed mode control signal 25 is deactivated, causing controller output enables 26a and 26b to activate and transceiver output enables to deactivate. PE and GR are now serviced by the local Bus Arbiter 12. RQ0 and RQ1 are inputs from Protocol Control 13 identifying the device that requires mastership of the System Bus 15. These two inputs are sent to both the Transceiver 16 (who passes the signals on to the Central Arbiter 18) and to the Bus Arbiter 12.

An advantage of the invention is the software portability which is provided by mode independent operation. Since the run-time software is identical in distributed mode and central mode; the drivers can be ported from one system to another system. Thus, electronic board designers who are using Bus Arbiter Circuit 12 and who have already designed their driver software are able to plug their software into any system. This

saves a lot of rewriting of codes which is one of the largest overheads in electronic board design.

Five registers are provided to facilitate software independence. These registers are message register 32, priority 0 register 33, priority 1 register 34, Logical Module control 30, and Logical Common Control 31.

FIG. 3 and 4 are flow diagrams illustrating the software independence capability of the invention. In both figures the steps written inside an octagon represent steps performed by the software executed by the module CPU 10.

FIG. 3 shows the functional steps followed by the invention when sending a general arbitration message. Software determines when general arbitration messages are sent. At Step 36 the software performs a write of the Send Message Register 32 this prompts the Bus Arbiter 12 to begin operation. At Step 37 the mode is checked by the Arbitration Protocol Sequencer 28. If the system is in central mode step 38 is to send a one byte arbitration message to the other modules in the system 19 . . . n. If the system is in distributed mode, step 39 is to send a two byte arbitration message to the other modules in the system 19 . . . n. Once the message is sent, the Bus Arbiter Circuit 12 issues an interrupt, Step 40, indicating that the arbitration message has been sent. The Bus Arbiter 12 is now ready to start again at Step 35 whenever software needs to send the next general arbitration message. As demonstrated by FIG. 3, the software interface points, Steps 36 and 40, are identical independent of the system mode; therefore, software independence is achieved.

FIG. 4 is also a flow diagram illustrating the software independence feature of the invention. FIG. 4 shows the functional steps followed by the invention when the task performed by software changes priority. The Bus Arbiter 12 performs a priority update when either Arbitration Priority 0 Register 33, or Arbitration Priority 1 Register 34, is written to via the local bus 11. At step 42 the software performs a write to either priority register 33 or 34. At Step 43 the Bus Arbiter 12 checks the mode by observing the central-arbiter bit in register 31. If the system is in distributed mode the Bus Arbiter Circuit 12 issues an interrupt at Step 48 to the CPU 10 informing the software that the priority has been updated.

If the system is in central mode Step 44 is determining which priority in the central arbiter circuit 18 needs to be updated. This decision is based upon which register (33 or 34) was written. If the Priority 1 register 34 was written then at Step 45 the Priority 1 update message is sent to the System Bus 15. If the Priority 0 register 33 was written then a Priority 0 update message is sent to the System Bus 15. At step 47 the Bus Arbiter 12 waits until the message has been sent to the Central Arbiter 18 over the System Bus 15. Once the message has been sent, the System Module 20 priorities are automatically updated in the Central Arbiter 18. At this point the Bus Arbiter Circuit 12 issues an interrupt at Step 48 to inform software that the priority has been updated. At this point the module is ready to perform a bus request at the new level. It is also ready to perform a new priority update starting at Step 41. The software interface points of writing to registers 33 or 34, Step 42, and issuing the interrupt, Step 48, are identical independent of the mode (distributed or central). Thus software independence is again achieved.

Bus Arbiter 12 supports a wide variety of configurations. Two possible configurations are shown in FIGS. 5 and 6. Additionally, hybrids of these configurations

may be devised by the system designer to meet specific design goals.

FIG. 5 shows a distributed mode only configuration. The arbitration speed of a distributed mode system is the slowest of the two configurations shown. In a distributed mode only configuration there are Bus Arbiters 12 on each module 52 . . . n and they all hook up to the system bus. This configuration would be used in situations where the computer is used in distributed arbitration operation only; such as for a fault tolerant system. In this configuration each Bus Arbiter 12 is used in distributed mode and competes for the System Bus 15 on behalf of its system module 52 . . . n.

FIG. 6 shows a programmable central arbiter system. There is a Central Arbiter 61 on one system module 62 and Bus Arbiters 12 on all of the other system modules 64 . . . n which program the Central Arbiter 61. All of the request and grant lines come into the Central Arbiter 61. Fault tolerance is improved by providing distributed arbitration, a fully redundant scheme that is transparent to normal operation of the host module. System operation time is reduced while operating in central mode.

Still other configurations could be comprehended by persons skilled in the art. For instance a system could be designed with all central arbiters, which could program each other and decide which central arbiter was going to act as master. Additionally the central arbiter could be on more than one system module for redundancy, however only one would be active at any given time.

While in accordance with the provisions and statutes there has been illustrated and described the best mode of the invention, certain changes may be made without departing from the spirit of the invention as set forth in a appended claims. Various modifications of the disclosed embodiment will become apparent to persons skilled in the art upon reference to the description of the invention. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

What is claimed is:

1. A system comprising:

- a system bus;
- system modules coupled to said system bus including a processor;
- a local bus coupled to said processor;
- arbitration circuitry coupled to said local bus and said system bus, said arbitration circuitry including
  - distributed mode operation circuitry which responds to a first signal allowing said arbitration circuitry to use distributed mode arbitration techniques to determine which system module gains access of said system bus,
  - central mode operation circuitry which responds to a second signal allowing a central arbiter to use central mode arbitration techniques to determine which system module gains access to said system bus, and

protocol control circuitry coupled to said arbitration circuitry, said system bus, and said local bus, for transferring information between said local bus and said system bus; said protocol control circuitry providing said first and second signal to said arbitration circuitry for selecting between distributed mode and said central mode operations.

2. The system of claim 1 wherein said arbitration circuitry further comprises:  
common hardware interface circuitry for enabling software independence for distributed mode and central mode operations.
3. The system of claim 1 further comprising:  
transceivers coupled to said arbitration circuitry and said protocol control circuitry for changing output signals from said arbitration circuitry to Backplane Transistor Logic (BTL) format used by said system bus and for allowing said arbitration circuitry output signals to be input onto said system bus.
4. The system of claim 1 wherein said arbitration circuitry comprises:  
an arbitration protocol sequencer coupled to said protocol control circuitry; and  
register circuitry coupled to said arbitration protocol sequencer and said local bus.
5. The system of claim 4 wherein the register circuitry comprises:  
a register for making dynamic mode changes possible by indicating whether the system is operating in central or distributed modes.
6. The system of claim 4 wherein the register circuitry comprises:  
a register for indicating whether or not said system module is master enabled.
7. The system of claim 4 wherein the register circuitry comprises:  
at least one register for storing an arbitration message.
8. The system of claim 4 wherein the register circuitry comprises:  
at least one register for dynamically storing a priority level.
9. The system of claim 4 wherein the register circuitry comprises:  
at least one register for storing the configuration, control, status, and test information needed for system bus arbitration.
10. The system of claim 1 wherein said system bus is a Futurebus+.
11. An arbiter circuit, comprising:  
an arbitration protocol sequencer for providing a common hardware protocol, between said arbiter circuit and any device desiring access to a system bus for distributed mode and central mode operation, said distributed mode operation using distributed mode arbitration techniques for allowing said arbiter circuit to determine which device gains access to said system bus, said central mode operation using central mode arbitration techniques for allowing a central arbiter to determine which device gains access to said system bus, said common hardware protocol provided by emulating a central mode arbitration sequence during distributed mode operation, and disabling itself and allowing a central mode arbiter to provide the central mode arbitration sequence during central mode operation; and  
register circuitry coupled to said arbitration protocol sequencer having common hardware interface circuitry for enabling software independence for distributed mode and central mode operations; wherein the mode of operation is determined by examining a bit in said register circuitry.
12. The circuit of claim 11 wherein said arbiter circuit performs central arbitration functions including: receiving bus mastership requests from all system modules

- requiring bus mastership; and granting bus mastership to any one of said system modules.
13. The circuit of claim 12 further including receiving priority updates from a system bus.
14. The arbiter circuit of claim 11 wherein said arbiter circuit is capable of dynamically switching from servicing a system module in central mode to servicing said system module in distributed mode.
15. The arbiter circuit of claim 11 wherein said arbiter circuit is capable of switching from servicing a system module in distributed mode to servicing said system module in central mode.
16. A method of communication between arbitration circuitry and its system module to utilize the arbitration process to determine which system module gains access to a system bus comprising the steps of:  
receiving service requests from said system module;  
determining whether the system is operating in distributed mode or central mode;  
sending a distributed mode arbitration message to said system module if the system is operating in distributed mode;  
sending a central mode arbitration message to said system module if the system is operating in central mode; and  
sending an indication to said system module that said operation is completed;  
wherein common hardware protocol is used for said central mode and distributed mode operations.
17. The method of claim 16 wherein said method is used to gain mastership of a system bus.
18. The method of claim 16 wherein said method is used to send messages.
19. The method of claim 16 wherein said method is used to update a priority.
20. A method of communication between arbitration circuitry and its system module to utilize the arbitration process to determine which system module gains access to a system bus comprising the steps of:  
receiving service requests from a system module;  
determining whether the system is operating in central mode or distributed mode;  
sending a distributed mode arbitration message to said system module if the system is operating in distributed mode;  
sending a central mode arbitration message to said system module if the system is operating in central mode; and  
sending an indication to said system module that said operation is completed;  
wherein common hardware interface circuitry enables software independence for distributed mode and central mode operations.
21. The method of claim 20 wherein said receiving and determining steps are used to gain mastership of a system bus.
22. The method of claim 20 wherein said receiving and determining steps are used to send messages.
23. The method of claim 20 wherein said method is used to update a priority.
24. A method of receiving arbitrated messages comprising the steps of:  
monitoring a system bus;  
determining mode of the system operation by examining the status of a bit located in a register;  
receiving and storing said arbitrated messages; and  
sending an indication to a system module that said arbitrated message has been received;

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said distributed mode operation using distributed mode operation techniques for allowing an arbiter circuit on each system module to determine which system module gains access to said system bus;  
 said central mode operation using central mode arbitration techniques for allowing a central arbiter to determine which system module gains access to said system bus;  
 wherein said determining, receiving, and sending steps are performed when the hardware interface circuitry is operating in both the distributed mode and central mode, and therefore, software independence is achieved.

25. A method of performing a priority update in an arbiter circuit when a system is operating in central mode and distributed mode comprising the steps of:  
 writing a priority value to a priority register;  
 determining whether said system is operating in distributed or central mode by examining the status of a bit located in a register;  
 issuing an interrupt signal to a local bus if said system is operating in distributed mode signifying that the priority is updated;  
 determining which priority is to be updated if said system is operating in central mode;  
 sending a priority update message appropriate for said determined priority if in central mode;  
 monitoring whether said message has been sent over a system bus; and

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issuing an interrupt if said message has been sent and if said system is operating in central mode.

26. The method of claim 25 wherein common hardware protocol is used for distributed mode and central mode operations.

27. The method of claim 25 wherein common hardware interface circuitry enables software independence for distributed mode and central mode.

28. A method of sending a general arbitration message to a module of a system from an arbiter circuit operating in distributed mode and central mode comprising the steps of:

writing said general arbitration message to a message register;  
 determining whether said system is operating in central mode or distributed mode;  
 sending a central mode arbitration message or distributed mode arbitration message to said module from said arbiter circuit in response to said determination; and  
 issuing an interrupt signal to a local bus indicating that one of said mode arbitration messages has been sent.

29. The method of claim 28 wherein common hardware protocol is used for distributed mode and central mode operations.

30. The method of claim 28 wherein common hardware interface circuitry enables software independence for distributed mode and central mode.

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# **EXHIBIT 2C**

## Provider Provisioned Virtual Private Network (VPN) Terminology

### Status of This Memo

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### Abstract

The widespread interest in provider-provisioned Virtual Private Network (VPN) solutions lead to memos proposing different and overlapping solutions. The IETF working groups (first Provider Provisioned VPNs and later Layer 2 VPNs and Layer 3 VPNs) have discussed these proposals and documented specifications. This has lead to the development of a partially new set of concepts used to describe the set of VPN services.

To a certain extent, more than one term covers the same concept, and sometimes the same term covers more than one concept. This document seeks to make the terminology in the area clearer and more intuitive.

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## 1. Introduction

A comparatively large number of memos have been submitted to the former PPVPN working group, and to the L2VPN, L3VPN, and PWE3 working groups, which all address the same problem space; provider provisioned virtual private networking for end customers. The memos address a wide range of services, but there is also a great deal of commonality among the proposed solutions.

This has led to the development of a partial set of new concepts used to describe this set of VPN services. To a certain extent, more than one term covers the same concept, and sometimes the same term covers more than one concept.

This document proposes a foundation for a unified terminology for the L2VPN and L3VPN working groups. In some cases, the parallel concepts within the PWE3 working group are used as references.

## 2. PPVPN Terminology

The concepts and terms in this list are gathered from Internet Drafts sent to the L2VPN and L3VPN mailing lists (earlier the PPVPN mailing list) and RFCs relevant to the L2VPN and L3VPN working groups. The focus is on terminology and concepts that are specific to the PPVPN area, but this is not strictly enforced; e.g., some concepts and terms within the PWE3 and (Generalized) MPLS areas are closely related. We've tried to find the earliest uses of terms and concepts.

This document is intended to fully cover the concepts within the core documents from the L2VPN and L3VPN working groups; i.e., [L3VPN-REQ], [L2VPN-REQ], [L3VPN-FRAME], [L2VPN], and [RFC3809]. The intention is to create a comprehensive and unified set of concepts for these documents and, by extension, for the entire PPVPN area. To do so, it is also necessary to give some of the development the concepts of the area have been through.

The document is structured in four major sections. Section 4 lists the different services that have been or will be specified. Section 5 lists the building blocks that are used to specify those services. Section 6 lists the functions needed in those services. Section 7 lists some typical devices used in customer and provider networks.

### 3. Provider Provisioned Virtual Private Network Services

In this section, we define the terminology that relates the set of services to solutions specified by the L2VPN and L3VPN working groups. The "pseudo wire" concept, which belongs to the PWE3 working group, is included for reference purposes. For requirements in provider provisioned VPNs, see [L3VPN-REQ].

All terms and abbreviations are listed together with a brief description of the service. The list is structured to give the more general information first and the more specific later. The names of services for which the IETF is working on solutions have been moved to the top of the list. Older and more dated terminology has been pushed toward the end of the list.

#### 3.1. Layer 3 VPN (L3VPN)

An L3VPN interconnects sets of hosts and routers based on Layer 3 addresses; see [L3VPN-FRAME].

#### 3.2. Layer 2 VPN (L2VPN)

Three types of L2VPNs are described in this document: Virtual Private Wire Service (VPWS) (Section 3.4); Virtual Private LAN Service (VPLS)(Section 3.3); and IP-only LAN-like Service (IPLS)(Section 3.5).

#### 3.3. Virtual Private LAN Service (VPLS)

A VPLS is a provider service that emulates the full functionality of a traditional Local Area Network (LAN). A VPLS makes it possible to interconnect several LAN segments over a packet switched network (PSN) and makes the remote LAN segments behave as one single LAN. For an early work on defining a solution and protocol for a VPLS, see [L2VPN-REQ], [VPLS-LDP], and [VPLS].

In a VPLS, the provider network emulates a learning bridge, and forwarding decisions are taken based on MAC addresses or MAC addresses and VLAN tag.

#### 3.4. Virtual Private Wire Service (VPWS)

A Virtual Private Wire Service (VPWS) is a point-to-point circuit (link) connecting two Customer Edge devices. The link is established as a logical through a packet switched network. The CE in the customer network is connected to a PE in the provider network via an Attachment Circuit (see Section 6.1); the Attachment Circuit is either a physical or a logical circuit.

The PEs in the core network are connected via a PW.

The CE devices can be routers, bridges, switches, or hosts. In some implementations, a set of VPWSs is used to create a multi-site L2VPN network. An example of a VPWS solution is described in [PPVPN-L2VPN].

A VPWS differs from a VPLS (Section 3.3) in that the VPLS is point to multipoint, while the VPWS is point to point. See [L2VPN].

### 3.5. IP-Only LAN-Like Service (IPLS)

An IPLS is very like a VPLS (see Section 3.3), except that

- o it is assumed that the CE devices (see Section 5.1) are hosts or routers, not switches,
- o it is assumed that the service will only have to carry IP packets, and supporting packets such as ICMP and ARP (otherwise layer 2 packets that do not contain IP are not supported); and
- o the assumption that only IP packets are carried by the service applies equally to IPv4 and IPv6 packets.

While this service is a functional subset of the VPLS service, it is considered separately because it may be possible to provide it by using different mechanisms, which may allow it to run on certain hardware platforms that cannot support the full VPLS functionality [L2VPN].

### 3.6. Pseudo Wire (PW)

The PWE3 working group within the IETF specifies the pseudo wire technology. A pseudo wire is an emulated point-to-point connection over a packet switched network that allows the interconnection of two nodes with any L2 technology. The PW shares some of the building blocks and architecture constructs with the point-to-multipoint solutions; e.g., PE (see Section 5.2) and CE (see Section 5.1). An early solution for PWs is described in [TRANS-MPLS]. Encapsulation formats readily used in VPWS, VPLS, and PWs are described in [ENCAP-MPLS]. Requirements for PWs are found in [RFC3916], and [PWE3-ARCH] presents an architectural framework for PWs.

### 3.7. Transparent LAN Service (TLS)

TLS was an early name used to describe the VPLS service. TLS has been replaced by VPLS, which is the current term.

### 3.8. Virtual LAN (VLAN)

The term VLAN was specified by IEEE 802.1Q; it defines a method of differentiating traffic on a LAN by tagging the Ethernet frames. By extension, VLAN is used to mean the traffic separated by Ethernet frame tagging or similar mechanisms.

### 3.9. Virtual Leased Line Service (VLLS)

The term VLLS has been replaced by term VPWS. VLLS was used in a now dated document intended to create metrics by which it should have been possible to compare different L2VPN solutions. This document has now expired, and the work has been terminated.

### 3.10. Virtual Private Network (VPN)

VPN is a generic term that covers the use of public or private networks to create groups of users that are separated from other network users and that may communicate among them as if they were on a private network. It is possible to enhance the level of separation (e.g., by end-to-end encryption), but this is outside the scope of IETF VPN working group charters. This VPN definition is from [RFC2764].

In the [L3VPN-FRAME], the term VPN is used to refer to a specific set of sites as either an intranet or an extranet that have been configured to allow communication. Note that a site is a member of at least one VPN and may be a member of many.

In this document, "VPN" is also used as a generic name for all services listed in Section 3.

### 3.11. Virtual Private Switched Network (VPSN)

The term VPSN has been replaced by the term VPLS. The requirements have been merged into the L3VPN [L3VPN-REQ] and L2VPN [L2VPN-REQ] requirements.

#### 4. Classification of VPNs

The terminology used in [RFC3809] is defined based on the figure below.

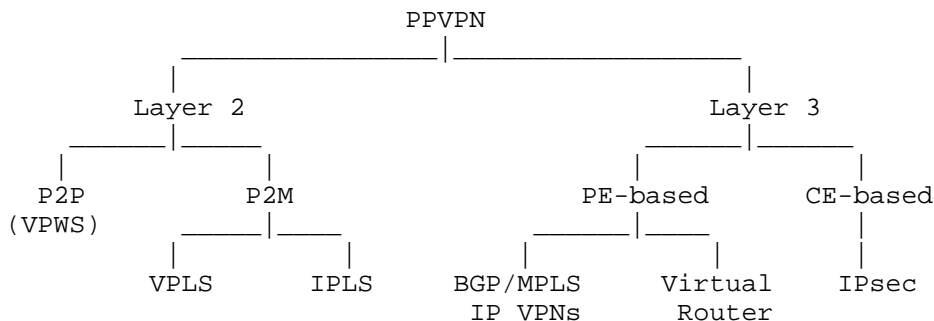


Figure 1

The figure above presents a taxonomy of PPVPN technologies. Some of the definitions are given below:

**CE-based VPN:** A VPN approach in which the shared service provider network does not have any knowledge of the customer VPN. This information is limited to CE equipment. All the VPN-specific procedures are performed in the CE devices, and the PE devices are not aware in any way that some of the traffic they are processing is VPN traffic (see also [L3VPN-FRAME]).

**PE-Based VPNs:** A Layer 3 VPN approach in which a service provider network is used to interconnect customer sites using shared resources. Specifically, the PE device maintains VPN state, isolating users of one VPN from users of another. Because the PE device maintains all required VPN states, the CE device may behave as if it were connected to a private network. Specifically, the CE in a PE-based VPN must not require any changes or additional functionality to be connected to a PPVPN instead of a private network.

The PE devices know that certain traffic is VPN traffic. They forward the traffic (through tunnels) based on the destination IP address of the packet, and optionally based on other information in the IP header of the packet. The PE devices are themselves the tunnel endpoints. The tunnels may make use of various encapsulations to send traffic over the SP network (such as, but not restricted to, GRE, IP-in-IP, IPsec, or MPLS tunnels) [L3VPN-FRAME].

Virtual Router (VR) style: A PE-based VPN approach in which the PE router maintains a complete logical router for each VPN that it supports. Each logical router maintains a unique forwarding table and executes a unique instance of the routing protocols. These VPNs are described in [L3VPN-VR].

BGP/MPLS IP VPNs: A PE-based VPN approach in which the PE router maintains a separate forwarding environment and a separate forwarding table for each VPN. In order to maintain multiple forwarding table instances while running only a single BGP instance, BGP/MPLS IP VPNs mark route advertisements with attributes that identify their VPN context. These VPNs are based on the approach described in [RFC2547bis].

RFC 2547 Style: The term has been used by the L3VPN to describe the extensions of the VPNs defined in the informational RFC 2547 [RFC2547]. This term has now been replaced by the term BGP/MPLS IP VPNs.

## 5. Building Blocks

Starting with specifications of L3VPNs (e.g., the 2547 specification [RFC2547] and [RFC2547bis] and Virtual Routers [L3VPN-VR]), a way of describing the building blocks and allocation of functions in VPN solutions was developed. The building blocks are often used in day-to-day talk as if they were physical boxes, common for all services.

However, for different reasons, this is an oversimplification. Any of the building blocks could be implemented across more than one physical box. How common the use of such implementations will be is beyond the scope of this document.

### 5.1. Customer Edge Device (CE)

A CE is the name of the device with the functionality needed on the customer premises to access the services specified by the former PPVPN working group in relation to the work done on L3VPNs [L3VPN-FRAME]. The concept has been modified; e.g., when L2VPNs and CE-based VPNs were defined. This is addressed further in the sub-sections of this section.

There are two different aspects that have to be considered in naming CE devices. One could start with the type of device that is used to implement the CE (see Section 5.1.1). It is also possible to use the service the CE provides whereby the result will be a set of "prefixed CEs", (see Section 5.1.2).

It is common practice to use "CE" to indicate any of these boxes, as it is very often unambiguous in the specific context.

#### 5.1.1. Device Based CE Naming

##### 5.1.1.1. Customer Edge Router (CE-R)

A CE-R is a router in the customer network interfacing the provider network. There are many reasons to use a router in the customer network; e.g., in an L3VPN using private IP addressing, this is the router that is able to do forwarding based on the private addresses. Another reason to require the use of a CE-R on the customer side is that one wants to limit the number of MAC-addresses that need to be learned in the provider network.

A CE-R could be used to access both L2 and L3 services.

##### 5.1.1.2. Customer Edge Switch (CE-S)

A CE-S is a service aware L2 switch in the customer network interfacing the provider network. In a VPWS or a VPLS, it is not strictly necessary to use a router in the customer network; a layer 2 switch might very well do the job.

#### 5.1.2. Service Based CE Naming

The list below contains examples of how different functionality has been used to name CEs. There are many examples of this type of naming, and we only cover the most frequently used functional names. As these are functional names, it is quite possible that on a single piece of equipment there are platforms for more than one type of function. For example, a router might at the same time be both a L2VPN-CE and a L3VPN-CE. It might also be that the functions needed for a L2VPN-CE or L3VPN-CE are distributed over more than one platform.

##### 5.1.2.1. L3VPN-CE

An L3VPN-CE is the device or set of devices on the customer premises that attaches to a provider provisioned L3VPN; e.g., a 2547bis implementation.

##### 5.1.2.2. VPLS-CE

A VPLS-CE is the device or set of devices on the customer premises that attaches to a provider provisioned VPLS.

#### 5.1.2.3. VPWS-CE

A VPWS-CE is the device or set of devices on the customer premises that attaches to a provider provisioned VPWS.

### 5.2. Provider Edge (PE)

A PE is the name of the device or set of devices at the edge of the provider network with the functionality that is needed to interface with the customer. Without further qualifications, PE is very often used for naming the devices since it is made unambiguous by the context.

In naming PEs there are three aspects that we need to consider, the service they support, whether the functionality needed for service is distributed across more than one device and the type of device they are build on.

#### 5.2.1. Device Based PE Naming

Both routers and switches may be used to implement PEs; however, the scaling properties will be radically different depending on which type of equipment is chosen.

##### 5.2.1.1. Provider Edge Router (PE-R)

A PE-R is a L3 device that participates in the PSN (see Section 8) routing and forwards packets based on the routing information.

##### 5.2.1.2. Provider Edge Switch (PE-S)

A PE-S is a L2 device that participates in for example a switched Ethernet taking forwarding decision packets based on L2 address information.

#### 5.2.2. Service Based PE Naming

##### 5.2.2.1. L3VPN-PE

An L3VPN-PE is a device or set of devices at the edge of the provider network interfacing the customer network, with the functionality needed for an L3VPN.

##### 5.2.2.2. VPWS-PE

A VPWS-PE is a device or set of devices at the edge of the provider network interfacing the customer network, with the functionality needed for a VPWS.

#### 5.2.2.3. VPLS-PE

A VPLS-PE is a device or set of devices at the edge of the provider network interfacing the customer network, with the functionality needed for a VPLS.

#### 5.2.3. Distribution Based PE Naming

For scaling reasons, in the VPLS/VPWS cases sometimes it is desired to distribute the functions in the VPLS/VPWS-PE across more than one device. For example, is it feasible to allocate MAC address learning on a comparatively small and inexpensive device close to the customer site, while participation in the PSN signalling and setup of PE to PE tunnels are done by routers closer to the network core.

When distributing functionality across devices, a protocol is needed to exchange information between the Network facing PE (N-PE) (see Section 5.2.3.1) and the User facing PE (U-PE) (see Section 5.2.3.2).

##### 5.2.3.1. Network Facing PE (N-PE)

The N-PE is the device to which the signalling and control functions are allocated when a VPLS-PE is distributed across more than one box.

##### 5.2.3.2. User Facing PE (U-PE)

The U-PE is the device to which the functions needed to take forwarding or switching decisions at the ingress of the provider network.

#### 5.3. Core

##### 5.3.1. Provider Router (P)

The P is defined as a router in the core network that does not have interfaces directly toward a customer. Therefore, a P router does not need to keep VPN state and is VPN unaware.

#### 5.4. Naming in Specific Internet Drafts

##### 5.4.1. Layer 2 PE (L2PE)

L2PE is the joint name of the devices in the provider network that implement L2 functions needed for a VPLS or a VPWS.

#### 5.4.2. Logical PE (LPE)

The term Logical PE (LPE) originates from a dated Internet Draft, "VPLS/LPE L2VPNs: Virtual Private LAN Services using Logical PE Architecture", and was used to describe a set of devices used in a provider network to implement a VPLS. In a LPE, VPLS functions are distributed across small devices (PE-Edges/U-PE) and devices attached to a network core (PE-Core/N-PE). In an LPE solution, the PE-edge and PE-Core can be interconnected by a switched Ethernet transport network or uplinks. The LPE will appear to the core network as a single PE. In this document, the devices that constitutes, the LPE are called N-PE and U-PE.

#### 5.4.3. PE-CLE

An alternative name for the U-PE suggested in the expired Internet Draft, "VPLS architectures".

#### 5.4.4. PE-Core

See the origins and use of this concept in Section 5.4.2.

#### 5.4.5. PE-Edge

See the origins and use of this concept in Section 5.4.2.

#### 5.4.6. PE-POP

An alternative name for the U-PE suggested in the expired Internet Draft, "VPLS architectures".

#### 5.4.7. VPLS Edge (VE)

The term VE originates from a dated Internet Draft on a distributed transparent LAN service and was used to describe the device used by a provider network to hand off a VPLS to a customer. In this document, the VE is called a VPLS-PE. This name is dated.

### 6. Functions

In this section, we have grouped a number of concepts and terms that have to be performed to make the VPN services work.

#### 6.1. Attachment Circuit (AC)

In a Layer 2 VPN the CE is attached to PE via an Attachment Circuit (AC). The AC may be a physical or logical link.

## 6.2. Backdoor Links

Backdoor Links are links between CE devices that are provided by the end customer rather than by the SP; they may be used to interconnect CE devices in multiple-homing arrangements [L3VPN-FRAME].

## 6.3. Endpoint Discovery

Endpoint discovery is the process by which the devices that are aware of a specific VPN service will find all customer facing ports that belong to the same service.

The requirements on endpoint discovery and signalling are discussed in [L3VPN-REQ]. It was also the topic in a now dated Internet Draft reporting from a design team activity on VPN discovery.

## 6.4. Flooding

Flooding is a function related to L2 services; when a PE receives a frame with an unknown destination MAC address, that frame is send out over (flooded) every other interface.

## 6.5. MAC Address Learning

MAC address learning is a function related to L2 services; when PE receives a frame with an unknown source MAC address, the relationship between that MAC-address and interface is learned for future forwarding purposes. In a layer 2 VPN solution from the L2VPN WG, this function is allocated to the VPLS-PE.

### 6.5.1. Qualified Learning

In qualified learning, the learning decisions at the U-PE are based on the customer Ethernet frame's MAC address and VLAN tag, if a VLAN tag exists. If no VLAN tag exists, the default VLAN is assumed.

### 6.5.2. Unqualified Learning

In unqualified learning, learning is based on a customer Ethernet frame's MAC address only.

## 6.6. Signalling

Signalling is the process by which the PEs that have VPNs behind them exchange information to set up PWS, PSN tunnels, and tunnel multiplexers. This process might be automated through a protocol or done by manual configuration. Different protocols may be used to establish the PSN tunnels and exchange the tunnel multiplexers.

## 7. 'Boxes'

We list a set of boxes that will typically be used in an environment that supports different kinds of VPN services. We have chosen to include some names of boxes that originate outside the protocol specifying organisations.

### 7.1. Aggregation Box

The aggregation box is typically an L2 switch that is service unaware and is used only to aggregate traffic to more function rich points in the network.

### 7.2. Customer Premises Equipment (CPE)

The CPE equipment is the box that a provider places with the customer. It serves two purposes: giving the customer ports to plug in to and making it possible for a provider to monitor the connectivity to the customer site. The CPE is typically a low cost box with limited functionality and, in most cases, is not aware of the VPN services offered by the provider network. The CPE equipment is not necessarily the equipment to which the CE functions are allocated, but it is part of the provider network and is used for monitoring purposes.

The CPE name is used primarily in network operation and deployment contexts and should not be used in protocol specifications.

### 7.3. Multi-Tenant Unit (MTU)

An MTU is typically an L2 switch placed by a service provider in a building where several customers of that service provider are located. The term was introduced in an Internet Draft specifying a VPLS solution with function distributed between the MTU and the PE in the context of a [VPLS].

The MTU device name is used primarily in network operation and deployment contexts and should not be used in protocol specifications, as it is also an abbreviation used for Maximum Transmit Units.

## 8. Packet Switched Network (PSN)

A PSN is the network through which the tunnels supporting the VPN services are set up.

### 8.1. Route Distinguisher (RD)

A Route Distinguisher [RFC2547bis] is an 8-byte value that, together with a 4 byte IPv4 address, identifies a VPN-IPv4 address family. If two VPNs use the same IPv4 address prefix, the PEs translate these into unique VPN-IPv4 address prefixes. This ensures that if the same address is used in two different VPNs, it is possible to install two completely different routes to that address, one for each VPN.

### 8.2. Route Reflector

A route reflector is a network element owned by a Service Provider (SP) that is used to distribute BGP routes to the SP's BGP-enabled routers [L3VPN-FRAME].

### 8.3. Route Target (RT)

A Route Target attribute [RFC2547bis] can be thought of as identifying a set of sites or, more precisely, a set of VRFs (see Section 8.9).

Associating a particular Route Target with a route allows that route to be placed in all VRFs used for routing traffic received from the corresponding sites.

A Route Target attribute is also a BGP extended community used in [RFC2547] and [BGP-VPN]. A Route Target community is used to constrain VPN information distribution to the set of VRFs. A route target can be perceived as identifying a set of sites or, more precisely, a set of VRFs.

### 8.4. Tunnel

A tunnel is connectivity through a PSN that is used to send traffic across the network from one PE to another. The tunnel provides a means to transport packets from one PE to another. Separation of one customer's traffic from another customer's traffic is done based on tunnel multiplexers (see Section 8.5). How the tunnel is established depends on the tunnelling mechanisms provided by the PSN; e.g., the tunnel could be based on the IP-header, an MPLS label, the L2TP Session ID, or the GRE Key field.

### 8.5. Tunnel Multiplexor

A tunnel multiplexor is an entity that is sent with the packets traversing the tunnel to make it possible to decide which instance of a service a packet belongs to and from which sender it was received. In [PPVPN-L2VPN], the tunnel multiplexor is formatted as an MPLS label.

### 8.6. Virtual Channel (VC)

A VC is transported within a tunnel and identified by its tunnel multiplexer. A virtual channel is identified by a VCI (Virtual Channel Identifier). In the PPVPN context, a VCI is a VC label or tunnel multiplexer, and in the Martini case, it is equal to the VCID.

### 8.7. VC Label

In an MPLS-enabled IP network, a VC label is an MPLS label used to identify traffic within a tunnel that belongs to a particular VPN; i.e., the VC label is the tunnel multiplexer in networks that use MPLS labels.

### 8.8. Inner Label

"Inner label" is another name for VC label (see Section 8.6).

### 8.9. VPN Routing and Forwarding (VRF)

In networks running 2547 VPN's [RFC2547], PE routers maintain VRFs. A VRF is a per-site forwarding table. Every site to which the PE router is attached is associated with one of these tables. A particular packet's IP destination address is looked up in a particular VRF only if that packet has arrived directly from a site that is associated with that table.

### 8.10. VPN Forwarding Instance (VFI)

VPN Forwarding Instance (VFI) is a logical entity that resides in a PE that includes the router information base and forwarding information base for a VPN instance [L3VPN-FRAME].

### 8.11. Virtual Switch Instance (VSI)

In a layer 2 context, a VSI is a virtual switching instance that serves one single VPLS [L2VPN]. A VSI performs standard LAN (i.e., Ethernet) bridging functions. Forwarding done by a VSI is based on MAC addresses and VLAN tags, and possibly on other relevant information on a per VPLS basis. The VSI is allocated to VPLS-PE or, in the distributed case, to the U-PE.

### 8.12. Virtual Router (VR)

A Virtual Router (VR) is software and hardware based emulation of a physical router. Virtual routers have independent IP routing and forwarding tables, and they are isolated from each other; see [L3VPN-VR].

## 9. Security Considerations

This is a terminology document and as such doesn't have direct security implications. Security considerations will be specific to solutions, frameworks, and specification documents whose terminology is collected and discussed in this document.

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